# UNIT – VI

**SAMPLING GATES AND LOGIC GATES**

### 6.1 IC families:

**comparison of the important characteristics of various IC logic families.**



* + 1. **CMOS inverter**
		2. **Tristate logic**
1. CMOS Inverter: It is complementary MOSFET obtained by using P-channel MOSPET and n-channel MOSFET simultaneously. The P and N channel are connected in series, their drains are connected together, output is taken from common drain point. Input is applied at common gate terminal. CMOS is very fast and consumes less power**.**



**Case 1**. When input Vi = 0. The  (Gate source) voltage of Q1 will be 0 volt, it will be off. But Q2 will be ON; Hence output will be equal to +VDD or logic 1.

**Case 2**. When input Vi = 1, The  (Gate source) voltage of Q2 will be 0 volt, it will be OFF, But Q1 will be ON. Hence output will be connected to•

ground or logic 0.

In this way, CMOS function as an inverter.

1. **Tri-state logic:** When there are three states i.e. state 0, state 1 and high impendence i.e. called Tri-state logic. High impedance is considered as state when no current pass through circuit. Although in state 0 and state 1 circuit functions and current flows through it.
	* Propagation delay is the average transition delay time for a pulse to propagate from input to output of a switching circuit.
	* Fan-in is the number of inputs to the gate which it can handle.
	* Fan-out is the number of loads the output of a gate can drive without effecting its operation.
	* Power dissipation is the supply voltage required by the gate to operate with 50% duty cycle at a given frequency
	* RTL, DTL, DTL are the logic families which are now obsolete.
	* TTL is the most widely used logic family.
	* TTL gates may be:
2. Totem pole
3. Open collector
4. Tri-state .
	* TTL is used in SSI and MSI Integrated circuits and is the fastest of all standard logic families.
	* Totem pole TTL has the advantage of high speed and low power dissipation but its disadvantage is that it cannot be wired ANDed because of current spikes generation.
	* Tri-state has three states : .
5. High
6. Low
7. High Impedance
	* ECL is the fastest of all logic families because its propagation delay is very small i.e. of about 2 nsec.
	* ECL can be wired ORed.
	* MOS logic is the simplest to fabricate.
	* MOS transistor can be connected as a resistor.
	* MOSFET circuitry are normally constructed from NMOS devices because they are 3 times faster than PMOS devices.
	* CMOS uses both P-MOS and N-MOS.
	* CMOS needs less power as compared to ECL as they need maximum power.
	* Both NMOS and PMOS are more economical than CMOS because of their greater packing densities.
	* Speed of CMOS gates increases with increase in VDD.
	* CMOS has large fan-out because of its low output resistance.

### Schematic of RTL NOR gate and explain its operation.

RTL was the first to introduced. RTL NOR gate is as shown in fig.



### Working:

**Case I:** When A = B = 0.

Both T1 and T2 transistors are in cut off state because the voltage is insufficient to drive the transistors i.e. VBE < 0.6 V: Thus, output Y will be high, approximately equal to supply voltage Vcc. As no current flows through Rc and drop across Rc is also zero.

Thus, Y = 1, when A = B = 0.

**Case II :** When A = 0 and B = 1 or A = 1 and B = 0.

The transistor whose input is high goes into saturation where as other will goes to off cut state. This positive input to transistor increases the voltage drop across the collector resistor and decreasing the positive output voltage.

Thus, Y = 0,when A= 0 and B = 1 or A = 1 and B = 0.

**Case III :** When A = B = 1**.** Both the transistors T1 and T2 goes into saturation and output voltage is equal to saturation voltage.

Thus, Y = 0,when A = B = 1 Truth Table



Which is the output of NOR gate.

### DCTL NAND gate with the help of suitable circuit diagram.

DCTL NAND gate circuit diagram is as shown:



### Working

**Case I:** When A = B = 0. Both transistors T1 and T2 goes to cut off state. As the voltage is not sufficient to drive the transistor into saturation. Thus, the output voltage equal to Vcc.

When A = B = 0, output Y = 1

**Case II:** When A = 0 and B = 1 or A = 1 and, B = 0. The corresponding transistor goes to cut off state and the output voltage equals to Vcc.

Thus, When A = 0 and B = 1 or A = 1 and B = 0, Output Y = 1.

**Case III:** When A = B = 1. Both transistors T1 and T2 goes into saturation state and output voltage is insufficient to consider as ‘1’

Thus when A B = 1, output Y = 0. Truth Table



Which is the output of NAND gate.

### Compare standard TTL, Low power TTL and high speed TTL logic families.



**characteristics and specification of CMOS.**

1 Power supply (VDD) = 3 — 15 Volts

1. Power dissipation (Pd) = 10 nW
2. Propagation delay (td) = 25 ns
3. Noise margine (NM) = 45% of VDD 5, Fan out (FO) = >50

### Two input ECL NOR gate

The circuit diagram of two input ECL NOR gate is as shown:



### Working

**Case I :** When A = B = 0, the reference voltage of T3 is more forward biased then T1 and T2. Thus, T3 is ON and T1, T2 remains OFF. The value of R1 is such-that the output of NOR gate is high .i.e. ‘1’.

**Case II:** When A = 1 or B = 1 or A = B = 1, the corresponding transistors are ON, as they are more forward biased that T3 and thus T3 is OFF. Which makes the NOR output to be low i.e. ‘0’.

This shows that the circuit works as a NOR gate.

### TTL inverter.

Tristate TTL inverter utilizer the high-speed operation of totem-pole arrangement while permitting outputs to be wired ANDed (connected together). It is called tristate TTL because it allows three possible output stages. HIGH, LOW and High-Impedance. We know that transistor T3 is ON when output is HIGH and T4 is ON when output is LOW. In the high impedance state both transistors, transistor T3 and T4 in the totem pole arrangement are med OFF. As a result the output is open or floating, it is neither LOW nor HIGH.

The above fig. shows the simplified tristate inverter. It has two inputs A and E. A is the normal logic input whereas E is an ENABLE input. When ENABLE input is HIGH, the circuit works as a normal inverter. Because when E is HIGH, the state-of the transistor T1 (either ON or OFF) depends on the logic input A and the additional component diode is open circuited as cathode is at logic HIGH. When ENABLE input is LOW, regardless of the state of logic input the base- emitter junction of T is forward biased and as a result it turns ON. This shunts the current through R1 away from T2 making it OFF. As T2 is OFF, there is no sufficient drive for T4 conduct and hence T4 turns OFF. The LOW at ENABLE input also forward biases diode D2, which shunt the current away from the base of T3, making it OFF. In this way, when ENABLE output is LOW, both transistors are OFF and output is at high impedance state.

### ECL OR gate

**ECL or gate :** Emitter-coupled logic (ECL) is the fastest of all logic families and thus it is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated. Here, rather than switching the transistors from ON to OFF and vice-versa, they are switched between cut-off and active regions. Propagation delays of less than 1 ns per gate have become possible in ECL.

Basically, ECL is realized using difference amplifier in which the emitters of the two transistors are connected and hence it referred to as emitter-coupled logic. A 3-input ECL gate is shown in Fig. (A) which has three parts. The middle part is the difference amplifier which performs the logic operation.



Emitter followers are used for d.c. level shifting of the outputs, so that V (0) and V (1) are same for the inputs and the outputs. Note that two output Y1 and Y2 are available in this circuit which are complementary. Y1. corresponds to OR logic and Y2 to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to T1 to get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the supply voltage is concerned. In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimize the effect of noise induced in the power supply and protection of the gate from an accidental short circuit developing between the output of a gate and ground. The voltage corresponding to V (0) and V (1) are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig. (B)



### Open collector TTL NAND gate and explain its operation

The circuit diagram of 2-input NAND gate open-collector TTL gate is as shown:



### Working:

**Case.1** : When A = 0,B = 0

When both inputs A and B are low, both functions of Q1 are forward biased and Q2 remains off. So no current flows through R4 and Q3 is also off and its collector voltage is equal to Vcc i.e. Y

= 1

**Case2 :** When A = 0, B = 1 and

**Case 3**: When A = 1, B = 0

When one input is high and. other is low, then one junction is forward biased so Q2 is off and Q3 is also off. So collector voltage is equal to Vcc i.e. Y = 1

**Case 4**: When A = 1, B = 1

When both inputs are high, Q1 is turned off and Q2 turned ‘ON’ Q3 goes into saturation and hence Y = 0. The open-collector output has main advantage that wired ANDing is possible in it. **TTL NAND gate**

Two input TTL NAND gate-is given in fig. (1). In this transistor T3 and T4 form a totem pole. Such type of configuration is called-as totem-pole output or active pull up output.



So, when A = 0 and B = 1 or (+5V). T1 conducts and T2 switch off. Since T2 is like an open switch, no current flows through it. But the current flows through the resistor R2 and into the base of transistor T3 to turn it ON. T4 remains OFF because there is no path through which it can receive base current. The output current flows through resistor R4 and diode D1. Thus, we get high’ output.

When both inputs are high i.e. A = B = 1 or (+ 5V), T2 is ON and it drives T4 turning it ON. It is noted that the voltage at the base of T3 equals the sum of the base to emitter drop of

T4 and  of T2.

The diode D1 does not allow base-emitter junction of T3 to be forward-biased and hence, T3 remains OFF when T4 is ON. Thus, we get low output.

It works as TTL NAND gate.

### Totem pole NAND gate

In TTL Totem pole NAND gate, multiple emitter transistor as input is used. The no. of inputs may be from 2 to 8 emitters. The circuit diagram is as shown



### Case 1:

When A = 0, B = 0

Now D1 and D2 both conduct, hence D3 will be off and make Q2 off. So its collector voltage rises and make Q3 ‘ON’ and Q4 off; Hence output at Y = 1 (High)

### Case 2 and Case 3:

If A = 0, B = 1 and A = 1, B=0

In both cases, the diode corresponding to low input will conduct and hence diode P3 will be OFF making Q2 OFF. In a similar way its collector voltage rises Q3 ‘ON’ and Q4 ‘OFF’. Hence output voltage Y = 1 (High).

**Case 4:** A = 1, B = 1

Both diodes D1 and D2 will be off. D3 will be ‘ON’ and Q2 will ‘ON’ making Q4 also ‘ON’. But Q3 will be ‘OFF’. So output voltage Y = 0.

All the four cases shows that circuit operates as a NAND gate.

Totem pole can’t be Wired ANDed due to current spike problem. The transistors used in circuits may get damaged over a period of time though not immediately. Sometimes voltage level rises high than the allowable.

These sampling gates help in selecting the transmission signal in a certain time interval, for which the output signal is same as input signal or zero otherwise. That time period is selected using a **control signal** or **selection signal**.

## 6.2 Sampling Gates

For a Sampling gate, the output signal must be same as the input or proportional to the input signal in a selected time interval and should be zero otherwise. That selected time period is called as **Transmission Period** and the other time period is called as **Non-transmission Period**. This is selected using a **control signal** indicated by VC. The following figure explain this point.



When the control signal VC is at V1, the sampling gate is closed and when VCis at V2, it is open. The pulse width Tg indicates the time period for which the gate pulse is applied.

### Types of Sampling Gates

The types of Sampling gates include −

* **Unidirectional sampling sgates** − These type of sampling gates can pass either positive or negative going pulses through them. They are constructed using diodes.
* **Bidirectional sampling gate** − These type of sampling gates can pass both positive and negative going pulses through them. They are constructed using either diodes or BJTs.

## Types of Switches Used

The sampling gates can be constructed using series or shunt switches. The time period for which the switch has to be open or close is determined by the gating pulse signal. These switches are replaced by active elements like diodes and transistors.

The following figure shows the block diagrams of sampling gates using series and shunt switches.



### Sampling Gate using a Series Switch

In this type of switch, if the switch S is closed, the output will be exactly equal or proportional to the input. That time period will be the **Transmission Period**.

If the switch S is open, the output will be zero or ground signal. That time period will be the **Non-transmission Period**.

### Sampling Gate using a Shunt Switch

In this type of switch, if the switch S is closed, the output will be zero or ground signal. That time period will be the **Non-transmission Period**.

If the switch S is open, the output will be exactly equal or proportional to the input. That time period will be the **Transmission Period**.

The sampling gates are entirely different from logic gates of digital circuits. They are also represented by pulses or voltage levels. But they are digital gates and their output is not the exact replica of the input. Whereas the sampling gate circuits are the analog gates whose output is exact replica of the input.

**unidirectional sampling gate**

A unidirectional sampling gate circuit consists of a capacitor C, a diode D and two resistors R1 and RL. The signal input is given to the capacitor and the control input is given to the resistor R1. The output is taken across the load resistor RL. The circuit is as shown below.



According to the functioning of a diode, it conducts only when the anode of the diode is more positive than the cathode of the diode. If the diode has positive signal at its input, it conducts. The time period in which the gate signal is ON, is the transmission period. Hence it is during that period in which the input signal is transmitted. Otherwise the transmission is not possible.

The following figure shows the time periods of the input signal and the gate signal.



The input signal is transmitted only for the time period during which gate is ON as shown in the figure.

From the circuit we have,

The anode of the diode is applied with the two signals (VS and VC). If the voltage at the anode is indicated as VP and the voltage at the cathode is indicated as VN then the output voltage is obtained as

Vo=VP=(VS+VC)>VNVo=VP=(VS+VC)>VN

So the diode is in forward biased condition.

VO=VS+V1>VNVO=VS+V1>VN

Then

VO=VSVO=VS

When V1 = 0,

Then

VO=VS+V1WhichmeansVO=VSVO=VS+V1WhichmeansVO=VS

Ideal value of V1 = 0.

So, if V1 = 0, the entire input signal appears at output. If the value of V1 is negative, then some of the input is lost and if V1 is positive, additional signal along with input appears at the output.

This whole thing happens during transmission period.

During non-transmission period,

VO=0VO=0

As diode is in reverse biased condition

When voltage on anode is less than voltage on cathode,

VS+VC<0VoltsVS+VC<0Volts

During non-transmission period,

VC=V2VC=V2

VS+V2<0VS+V2<0

Magnitude of V2 should be very high than Vs.

|V2|≫VS|V2|≫VS

Because for the diode to be in reverse bias, the sum of the voltages VS and VCshould be negative. VC (which is V2 now) should be as negative as possible so that though VS is positive, the sum of both the voltages should yield a negative result.

## Pedestal Reduction

While going through different types of sampling gates and the outputs they produce, we have come across an extra voltage level in the output waveforms called as **Pedestal**. This is unwanted and creates some noise.

### Reduction of Pedestal in a Gate circuit

The difference in the output signals during transmission period and non-transmission period though the input signals is not applied, is called as **Pedestal**. It can be a positive or a negative pedestal.

Hence it is the output observed because of the gating voltage though the input signal is absent. This is unwanted and has to be reduced. The circuit below is designed for the reduction of pedestal in a gate circuit.



When the control signal is applied, during the transmission period i.e. at V1, Q1 turns ON and Q2 turns OFF and the VCC is applied through RC to Q1. Whereas during the nontransmission period i.e. at V2, Q2 turns ON and Q1turns OFF and the VCC is applied through RC to Q2. The base voltages –VBB1and –VBB2 and the amplitude of gate signals are adjusted so that two transistor currents are identical and as a result the quiescent output voltage level will remain constant.

If the gate pulse voltage is large compared with the VBE of the transistors, then each transistor is biased far below cut off, when it is not conducting. So, when the gate voltage appears, Q2 will be driven into cut off before Q1 starts to conduct, whereas at the end of the gate, Q1 will be driven to cut off before Q2 starts to conduct.

The figure below explains this in a better fashion.



Hence the gate signals appear as in the above figure. The gated signal voltage will appear superimposed on this waveform. These spikes will be of negligible value if the gate waveform rise time is small compared with the gate duration.

There are few **drawbacks** of this circuit such as

* Definite rise and fall times, result in sharp spikes
* The continuous current through RC dissipates lot of heat
* Two bias voltages and two control signal sources (complement to each other) make the circuit complicated.

## Four Diode Bidirectional Sampling Gate

Bidirectional sampling gate circuit is made using diodes also. A two diode bidirectional sampling gate is the basic one in this model. But it has few disadvantages such as

* It has low gain
* It is sensitive to the imbalances of control voltage
* Vn (min) may be excessive
* Diode capacitance leakage is present

A four diode bidirectional sampling gate was developed, improving these features. A two bidirectional sampling gate circuit was improved adding two more diodes and two balanced voltages +v or –v to make the circuit of a four diode bidirectional sampling gate as shown in the figure.



The control voltages VC and –VC reverse bias the diodes D3 and D4respectively. The voltages +v and –v forward bias the diodes D1 and D2respectively. The signal source is coupled to the load through the resistors R2and the conducting diodes D1 and D2. As the diodes D3 and D4 are reverse biased, they are open and disconnect the control signals from gate. So, an imbalance in control signals will not affect the output.

When the control voltages applied are Vn and –Vn, then the diodes D3 and D4conduct. The points P2 and P1 are clamped to these voltages, which make the diodes D1 and D2 revere biased. Now, the output is zero.

## Applications of Sampling Gates

There are many applications of sampling gate circuits. The most common ones are as follows −

* Sampling scopes
* Multiplexers
* Sample and hold circuits
* Digital to Analog Converters
* Chopped Stabilizer Amplifiers