Unit – IV

Objectives:

- To implement various switching functions using PLDs.
- To understand different logic families and their characteristics.

Syllabus:

Introduction of Programmable Logic Devices(PLD's):
PROM, PAL, PLA-Basics structures, realization of Boolean function with PLDs, programming tables of PLDs,merits & demerits of PROM, PAL, PLA comparison, realization of Boolean functions using PROM, PAL, PLA, programming tables of PROM, PAL, PLA.

Outcomes:

Students will be able to
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- Realize switching functions using PROM, PLA and PAL.
- Compare various types of PLDs.

Learning Material

Programmable Logic Devices

- A Programmable Logic Device is an integrated circuit with internal logic gates and interconnects. These gates can be connected to obtain the required logic configuration through a program (HDL).
- The term "programmable" means changing either hardware or software configuration of an internal logic and interconnects.
- The configuration of the internal logic is done by the user.
- PROM, EPROM, PAL, PLA, GAL etc. are examples of Programmable Logic devices.
- Programmable Read Only Memory (PROM) - a fixed array of AND gates and a programmable array of OR gates
- Programmable Array Logic (PAL) - a programmable array of AND gates feeding a fixed array of OR gates.
- Programmable Logic Array (PLA) - a programmable array of AND gates feeding a programmable array of OR gates.

Programmable Array Logic (PAL)

- The PAL structure consists of <u>programmable</u> set of ANDs combined with <u>fixed</u> ORs which is shown in the figure 4.1 below

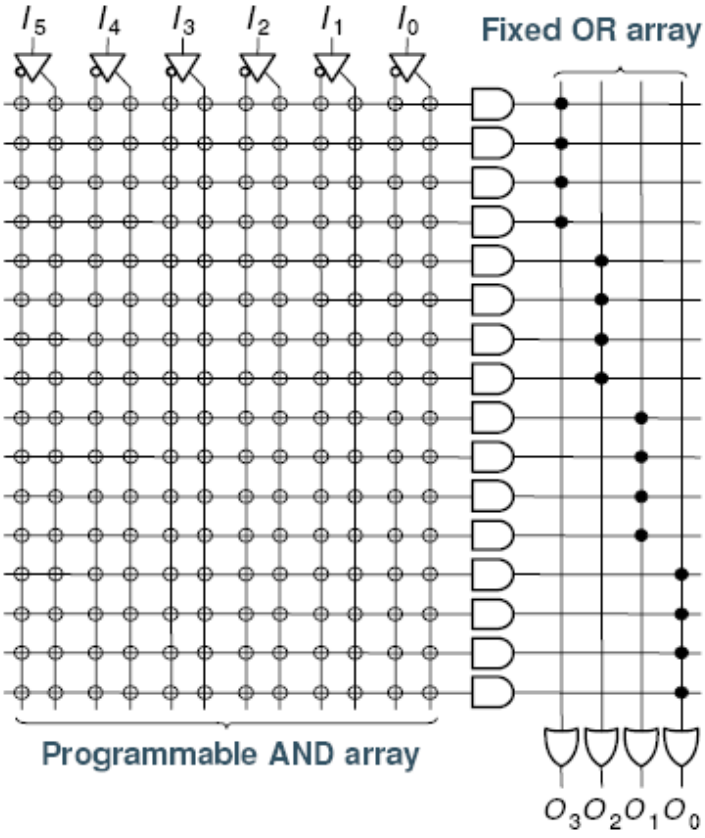

Fig. 4.1: PAL Structure

- Disadvantage
    - ROM guaranteed to implement any M functions of N inputs. PAL may have too few inputs to the OR gates.
- Advantages
    - For given internal complexity, a PAL can have larger N and M
    - Some PALs have outputs that can be complemented, adding POS functions
    - No multilevel circuit implementations in ROM (without external connections from output to input).
    - PAL has outputs from OR terms as internal inputs to all AND terms, making implementation of multi-level circuits easier.
- Example
    - Implement the following functions using PAL which is shown in fig 4.3
    - $F_1 = A'B' + C'$, $F_2 = A'BC' + AC + AB'$, $F_3 = A'I_4 + BI_4 + F_1$,
    - $F_4 = AB + CI_4 + F_1'$

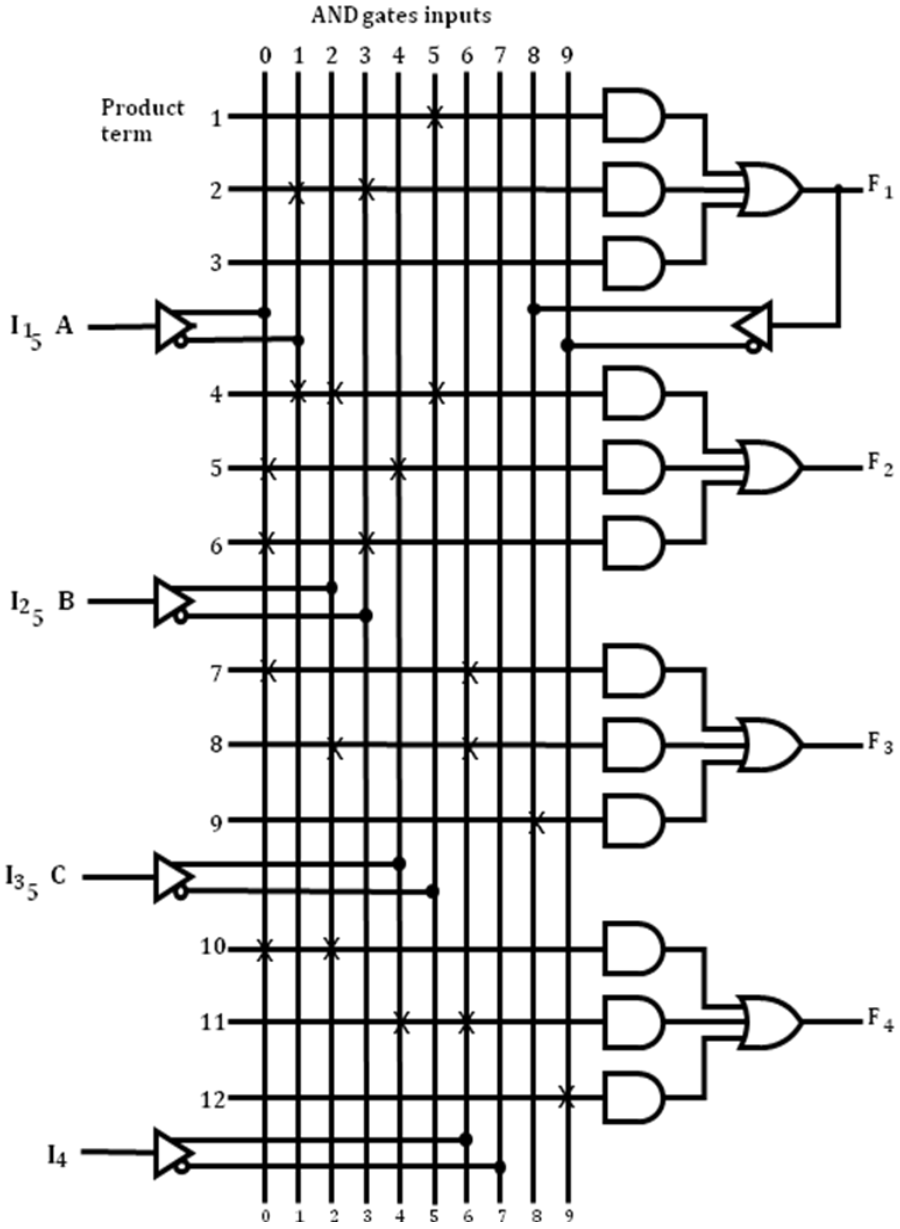

Fig 4.3: PAL example

Programmable Logic Array (PLA)

- The PLA structure consists of programmable set of ANDs combined with a programmable set of ORs which is shown in the figure 4.2 below
- Advantages
  - A PLA can have large N and M permitting implementation of equations that are impractical for a ROM (because of the number of inputs, N, required
  - A PLA has all of its product terms connectable to all outputs, overcoming the problem of the limited inputs to the PAL Ors
  - Some PLAs have outputs that can be complemented, adding POS functions
- Disadvantage
  - Often, the product term count limits the application of a PLA. Two-level multiple-output optimization reduces the number of product terms in an implementation, helping to fit it into a PLA.

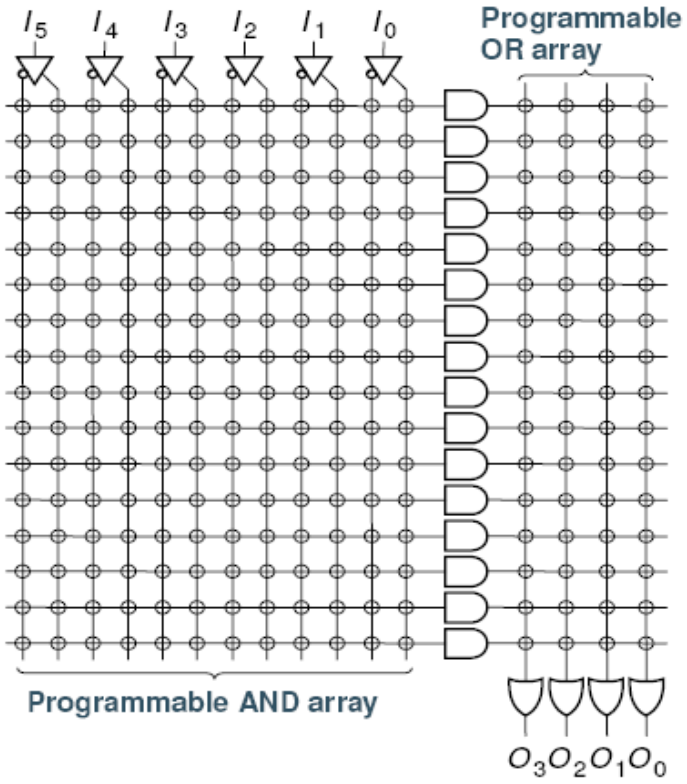

Fig. 4.2: PLA Structure

- Example
  - Implement the following functions using PLA which is shown in fig 4.4
  - $F_0 = ABC$, $F_1 = ABC + A'B'$, $F_2 = ABC + B'C' + A'C'$

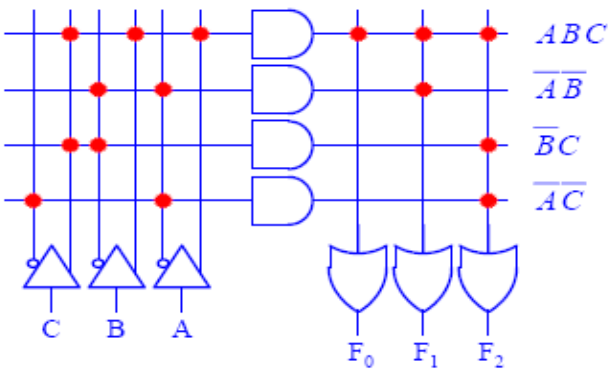

Fig 4.4: PLA example

Programmable Read Only Memory (PROM)

- First type of user-programmable chip and One-time programmable
- Device has a fixed, fully decoded AND plane and a programmable OR plane
- A logic circuit can be implemented by using the PROM's address lines as the circuit's inputs and the circuit's outputs are then defined by the stored bits, which are shown in figure 4.5 below.

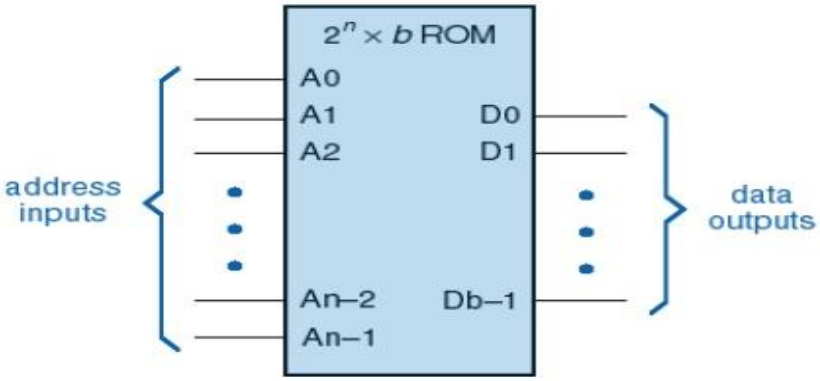

Fig 4.5: Structure of PROM

- Example
  - A 8 X 4 PROM (N = 3 input lines, M= 4 output lines)
  - F0 = ∑m(1,5,7) , F1 = ∑m(1,4) , F2=∑m(0, 7) , F3=∑m(2,5,7)
  - The fixed "AND" array is a "decoder" with 3 inputs and 8 outputs implementing minterms which is shown in fig 4.6 below

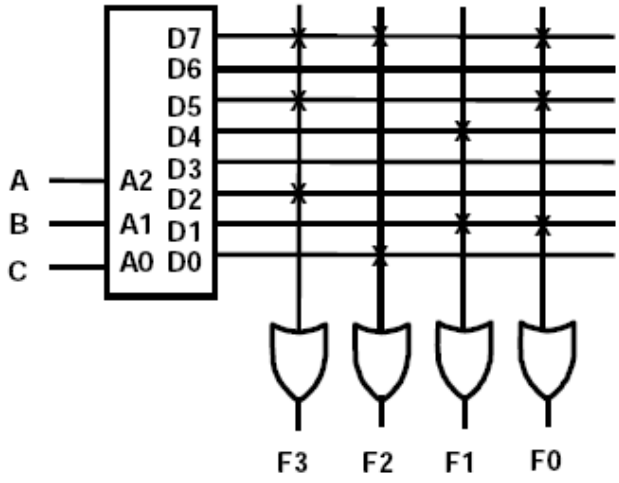

Fig 4.6: PROM example

Comparison of PROM, PLA and PAL

PROM	PLA	PAL
AND array is fixed and OR array is programmable.	Both AND and OR arrays are programmable.	OR array is fixed and AND array is programmable.
Cheaper and simple to use.	Costliest and complex than PAL and PROMs,	Cheaper and simpler.
Ail minterms are decoded.	AND array can be programmed to get desired minterms.	AND array can be programmed to get desired minterms.
Onfy Boolean functions in Standard SOP form can be implemented using PROM	Any Boolean functions In SOP form can be implemented using PLA.	Any Boolean functions In SOP form can be implemented using PLA.

Assignment-Cum-Tutorial Questions

A. Questions testing the remembering / understanding level of students

I) Objective Questions

1. PALs tend to execute _____ logic.
A. SAP B.SOP C.PLA D. SPD

2. A _____ PLD consists of a programmable array of AND gates that connects to a fixed array of OR gates and is usually OTP.

3. By adding an OR gate to a simple programmable logic device (SPLD) the foundation for a _____ PLD is made possible.

4. Which type of PLD should be used to program basic logic functions?

II) Descriptive Questions

1. Give the classification of PLDs with respect to their programmability.
2. Explain the internal structure of PROM.
3. What is programmable logic array? How it differs from PROM?
4. Give the comparison between PROM, PLA and PAL

B. Question testing the ability of students in applying the concepts.

I) Objective Questions

1) For designing a 4-variable combinational circuit, a designer must use a
A. ROM with atleast 16 locations
B. PLA with atleast 32 product terms
C. PLA with atleast 16 product terms
D. PLA with atleast 16 product terms and 16 input OR gate

2) A 32x10 ROM contains a decoder of size
A. 5x32 B. 32x32 C.32x10 D. 10x32

3. Once a PAL has been programmed:
A. it cannot be reprogrammed. B. its outputs are only active HIGHs
C. its outputs are only active LOWs D. its logic capacity is lost

4. What do the Programmable Logic Devices (PLDs) designed especially for the combinational circuits comprise?
A. Only gates B. Only flip flops C. Both a and b D. None of the above

5. Which among the following statement/s is/are not an/the advantage/s of Programmable Logic Devices (PLDs)?
A. Short design cycle B. increased space requirement
C. Increased switching speed D. All of the above

II) Descriptive Questions

1. Four 4-variable functions are defined by the following equations:
   F1(A,B, C,D) = ∑m (2, 3, 6, 7, 11, 15)
   F2(A,B, C,D) = ∑m (0, 4, 8, 9, 11, 15)
   F3(A,B,C,D) = ∑m (1,3,5,7,10,11)
   F4(A,B,C,D) = ∑m (0, 2, 4, 6, 8, 9, 11, 12, 13, 15)
   Show how these functions can be implemented on a PLA having an 8*8 AND array and a 4*8 OR array.
2. Implement 3-bit binary to gray code converter using PROM
3. Using PAL, implement full adder digital circuit
4. Implement BCD to seven segment display using PLA

C. Questions testing the analyzing / evaluating ability of students

1. Design sequence detector 1101 using PLA and D-flip flops.
2. Derive the PLA programming table for the combinational circuit that squares a 3 bit number.
3. Design a combinational logic circuit using ROM. The circuit accepts BCD number and generates an output binary number equal to the 2's complement of the input number.
4. Implement 8:3 priority encoder using PAL.