UNIT-2

DIGITAL MODULATION TECHNIQUES

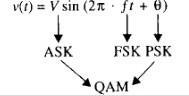
Digital Modulation provides more information capacity, high data security, quicker system availability with great quality communication. Hence, digital modulation techniques have a greater demand, for their capacity to convey larger amounts of data than analog ones.

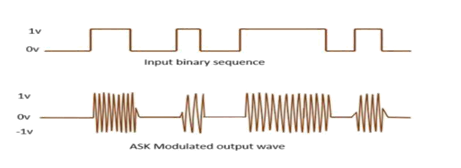
There are many types of digital modulation techniques and we can even use a combination of these techniques as well. In this chapter, we will be discussing the most prominent digital modulation techniques.

if the information signal is digital and the amplitude (lV of the carrier is varied proportional to the information signal, a digitally modulated signal called amplitude shift keying (ASK) is produced.

If the frequency (f) is varied proportional to the information signal, frequency shift keying (FSK) is produced, and if the phase of the carrier (0) is varied proportional to the information signal,

phase shift keying (PSK) is produced. If both the amplitude and the phase are varied proportional to the information signal, quadrature amplitude modulation (QAM) results. ASK, FSK, PSK, and QAM are all forms of digital modulation:





a simplified block diagram for a digital modulation system.

Amplitude Shift Keying

The amplitude of the resultant output depends upon the input data whether it should be a zero level or a variation of positive and negative, depending upon the carrier frequency.

Amplitude Shift Keying (ASK) is a type of Amplitude Modulation which represents the binary data in the form of variations in the amplitude of a signal.

Following is the diagram for ASK modulated waveform along with its input.

Any modulated signal has a high frequency carrier. The binary signal when ASK is modulated, gives a zero value for LOW input and gives the carrier output for HIGH input. Mathematically, amplitude-shift keying is



where vask(t) = amplitude-shift keying wave

vm(t) = digital information (modulating) signal (volts)

A/2 = unmodulated carrier amplitude (volts)

ωc= analog carrier radian frequency (radians per second, 2πfct)

In above Equation, the modulating signal [vm(t)] is a normalized binary waveform, where + 1 V = logic 1 and -1 V = logic 0. Therefore, for a logic 1 input, vm(t) = + 1 V, Equation 2.12 reduces to



Mathematically, amplitude-shift keying is (2.12) where vask(t) = amplitude-shift keying wave vm(t) = digital information (modulating) signal (volts) A/2 = unmodulated carrier amplitude (volts)

ωc= analog carrier radian frequency (radians per second, 2πfct) In Equation 2.12, the modulating signal [vm(t)] is a normalized binary waveform, where + 1 V = logic 1 and -1 V = logic 0. Therefore, for a logic 1 input, vm(t) = + 1 V, Equation 2.12 reduces to and for a logic 0 input, vm(t) = -1 V,Equation reduces to



Thus, the modulated wave vask(t),is either A cos(ωct) or 0. Hence, the carrier is either "on “or "off," which is why amplitude-shift keying is sometimes referred to as on-off keying (OOK).

it can be seen that for every change in the input binary data stream, there is one change in the ASK waveform, and the time of one bit (tb) equals the time of one analog signaling element (t,).

B = fb/1 = fb baud = fb/1 = fb

Example :

Determine the baud and minimum bandwidth necessary to pass a 10 kbps binary signal using amplitude shift keying. 10Solution For ASK, N = 1, and the baud and minimum bandwidth are determined from Equations 2.11 and 2.10, respectively:

B = 10,000 / 1 = 10,000

baud = 10, 000 /1 = 10,000

The use of amplitude-modulated analog carriers to transport digital information is a relatively low-quality, low-cost type of digital modulation and, therefore, is seldom used except for very low-speed telemetry circuits.

ASK TRANSMITTER:





The input binary sequence is applied to the product modulator. The product modulator amplitude modulates the sinusoidal carrier .it passes the carrier when input bit is ‘1’ .it blocks the carrier when input bit is ‘0.’

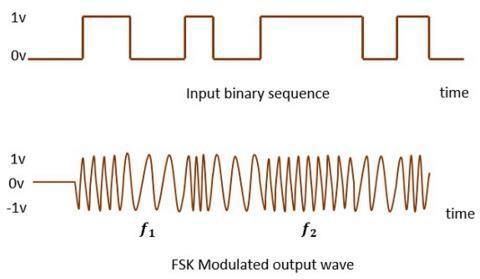
Coherent ASK DETECTOR:

FREQUENCYSHIFT KEYING

The frequency of the output signal will be either high or low, depending upon the input data applied.

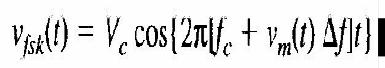
Frequency Shift Keying (FSK) is the digital modulation technique in which the frequency of the carrier signal varies according to the discrete digital changes. FSK is a scheme of frequency modulation.

Following is the diagram for FSK modulated waveform along with its input.



The output of a FSK modulated wave is high in frequency for a binary HIGH input and is low in frequency for a binary LOW input. The binary 1s and 0s are called Mark and Space frequencies.

FSK is a form of constant-amplitude angle modulation similar to standard frequency modulation (FM) except the modulating signal is a binary signal that varies between two discrete voltage levels rather than a continuously changing analog waveform.Consequently, FSK is sometimes called *binary FSK* (BFSK). The general expression for FSK is



where

vfsk(t) = binary FSK waveform

Vc *=* peak analog carrier amplitude (volts)

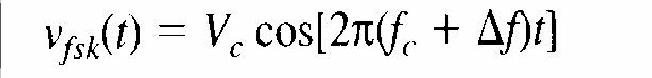
*fc =* analog carrier center frequency (hertz)

f=peak change (shift)in the analog carrier frequency(hertz)

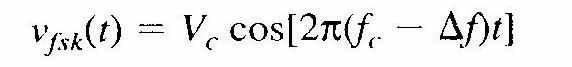
vm(t) = binary input (modulating) signal (volts)

From Equation 2.13, it can be seen that the peak shift in the carrier frequency ( f) is proportional to the amplitude of the binary input signal (vm[t]), and the direction of the shift is determined by the polarity.

The modulating signal is a normalized binary waveform where a logic 1 = + 1 V and a logic 0 = -1 V. Thus, for a logic l input, vm(t) = + 1, Equation 2.13 can be rewritten as



For a logic 0 input, vm(t) = -1, Equation becomes



With binary FSK, the carrier center frequency (fc) is shifted (deviated) up and down in the frequency domain by the binary input signal as shown in Figure 2-3.



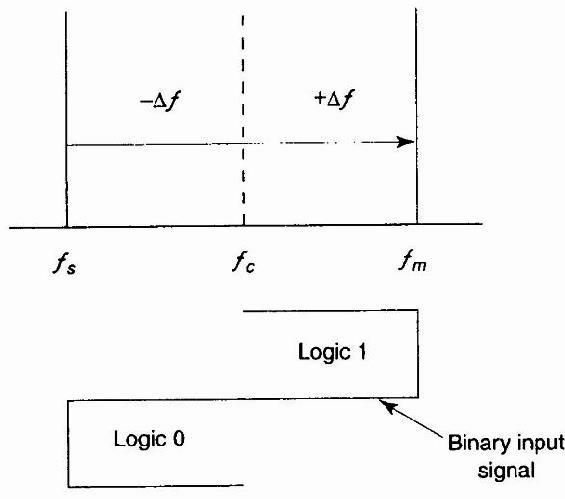


FIGURE: FSK in the frequency domain

As the binary input signal changes from a logic 0 to a logic 1 and vice versa, the output frequency shifts between two frequencies: a mark, or logic 1 frequency (fm), and a space, or logic 0 frequency (f*s*). The mark and space frequencies are separated from the carrier frequency by the peak frequency deviation ( f) and from each other by 2 f.

Frequency deviation is illustrated in Figure 2-3 and expressed mathematically as

|  |  |  |
| --- | --- | --- |
|  | f = |fm – fs| / 2 | (2.14) |
| where | f *=* fre quency deviation (hertz) |  |

|fm – fs| = absolute difference between the mark and space frequencies (hertz)

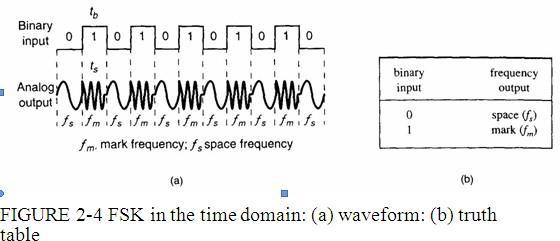
Figure 2-4a shows in the time domain the binary input to an FSK modulator and the corresponding FSK output.

When the binary input *(fb)* changes from a logic 1 to a logic 0 and vice versa, the FSK output frequency shifts from a mark ( f*m*) to a space (f*s*) frequency and vice versa.

In Figure 2-4a, the mark frequency is the higher frequency *(fc* *+* f) and the space frequency is the lower frequency (fc - f), although this relationship could be just the opposite.

Figure 2-4b shows the truth table for a binary FSK modulator. The truth table shows the input and output possibilities for a given digital modulation scheme.





FSK Bit Rate, Baud, and Bandwidth

In Figure 2-4a, it can be seen that the time of one bit *(tb)* is the same as the time the FSK output is a mark of space frequency *(t*s*).* Thus, the bit time equals the time of an FSK signaling element, and the bit rate equals the baud.

The baud for binary FSK can also be determined by substituting N *=* 1 in Equation 2.11:

baud = fb / 1 = fb

The minimum bandwidth for FSK is given as

B= |(fs – fb) – (fm – fb)|

=|(fs– fm)| + 2fb

and since |(fs– fm)| equals 2 f*,* the minimum bandwidth can be approximated as

|  |  |
| --- | --- |
| B= 2( f + fb) | (2.15) |

where

B= minimum Nyquist bandwidth (hertz)

f*=* frequency deviation |(fm– fs)| (hertz)

*fb =* input bit rate (bps)

Example 2-2

Determine (a) the peak frequency deviation, (b) minimum bandwidth, and (c) baud for a binary FSK signal with a mark frequency of 49 kHz, a space frequency of 51 kHz, and an input bit rate of 2 kbps.

Solution

a. The peak frequency deviation is determined from Equation 2.14:

f= |149kHz - 51 kHz| / 2 =1 kHz

b. The minimum bandwidth is determined from Equation 2.15:

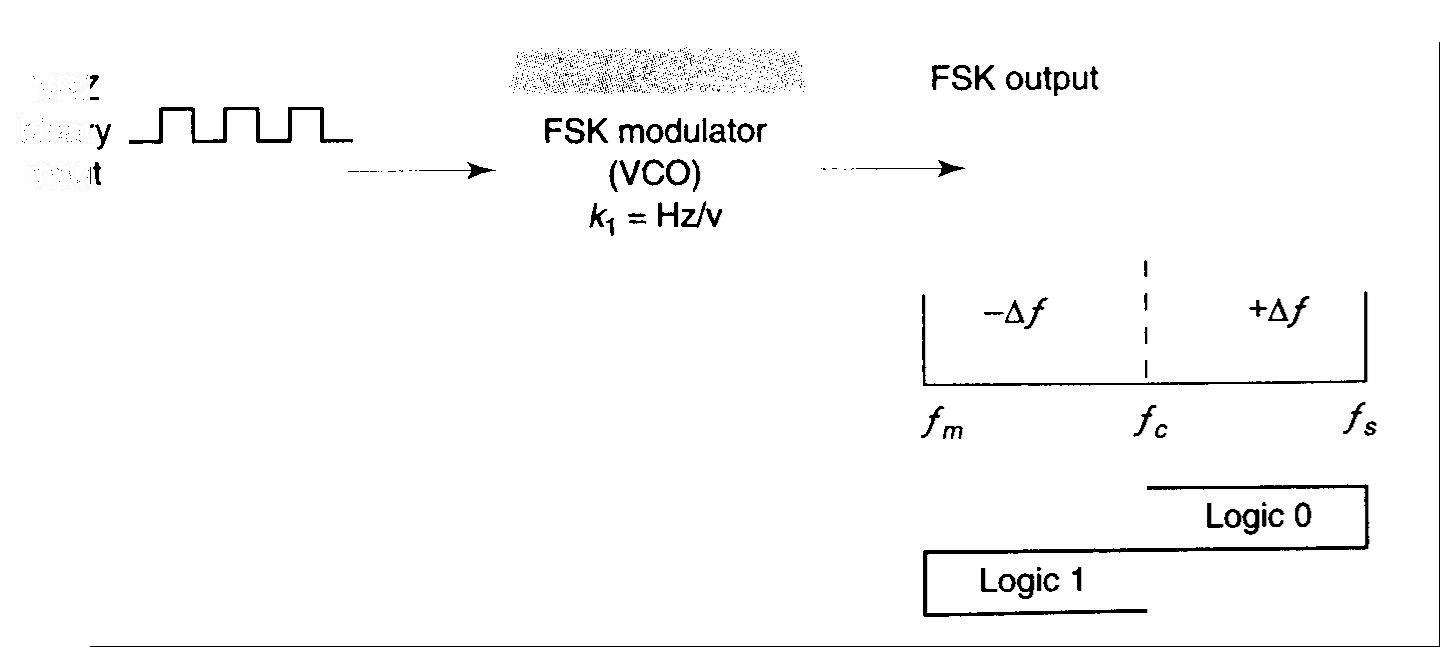
B = 2(100+ 2000)

=6 kHz

c. For FSK, *N =* 1, and the baud is determined from Equation 2.11 as baud = 2000 / 1 = 2000

FSK TRANSMITTER:

Figure 2-6 shows a simplified binary FSK modulator, which is very similar to a conventional FM modulator and is very often a voltage-controlled oscillator (VCO).The center frequency (fc) is chosen such that it falls halfway between the mark and space frequencies.



A logic 1 input shifts the VCO output to the mark frequency, and a logic 0 input shifts the VCO output to the space frequency. Consequently, as the binary input signal changes back and forth between logic 1 and logic 0 conditions, the VCO output shifts or deviates back and forth between the mark and space frequencies.

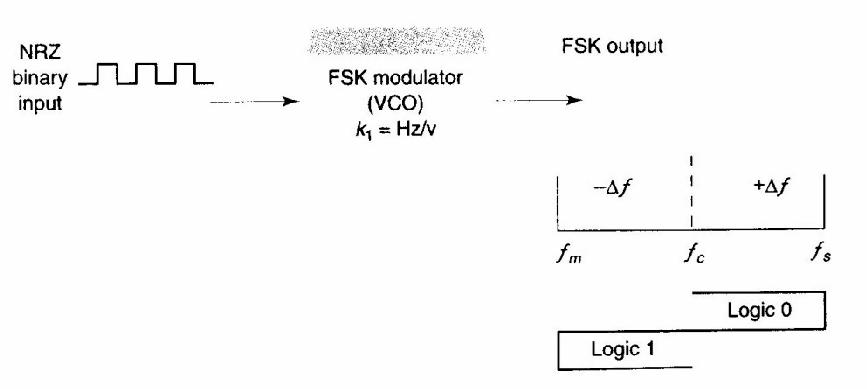


FIGURE 2-6 FSK modulator

A VCO-FSK modulator can be operated in the sweep mode where the peak frequency deviation is simply the product of the binary input voltage and the deviation sensitivity of the VCO.

With the sweep mode of modulation, the frequency deviation is expressed mathematically as

|  |  |
| --- | --- |
| *f = vm(t)kl* | (2-19) |

vm(t) = peak binary modulating-signal voltage (volts)

*kl* = deviation sensitivity (hertz per volt).

FSK Receiver

FSK demodulation is quite simple with a circuit such as the one shown in Figure 2-7.

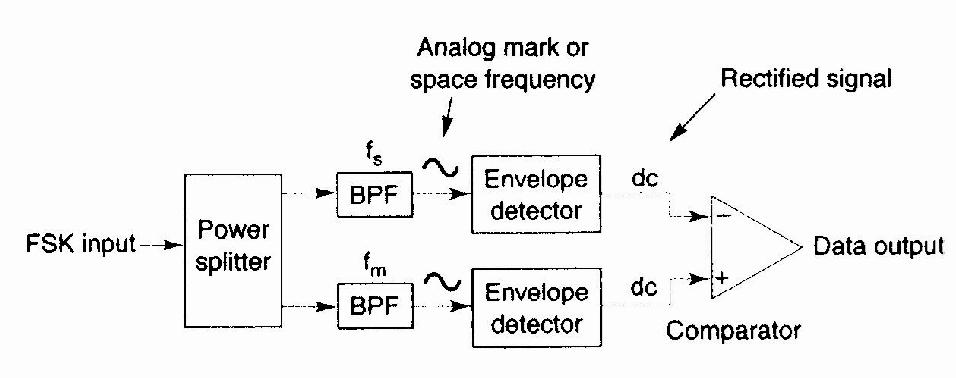


FIGURE 2-7 Noncoherent FSK demodulator

The FSK input signal is simultaneously applied to the inputs of both bandpass filters (BPFs) through a power splitter.The respective filter passes only the mark or only the space frequency on to its respective envelope detector.The envelope detectors, in turn, indicate the total power in each passband, and the comparator responds to the largest of the two powers.This type of FSK detection is referred to as noncoherent detection.

Figure 2-8 shows the block diagram for a coherent FSK receiver.The incoming FSK signal is multiplied by a recovered carrier signal that has the exact same frequency and phase as the transmitter reference.

However, the two transmitted frequencies (the mark and space frequencies) are not generally continuous; it is not practical to reproduce a local reference that is coherent with both of them. Consequently, coherent FSK detection is seldom used.

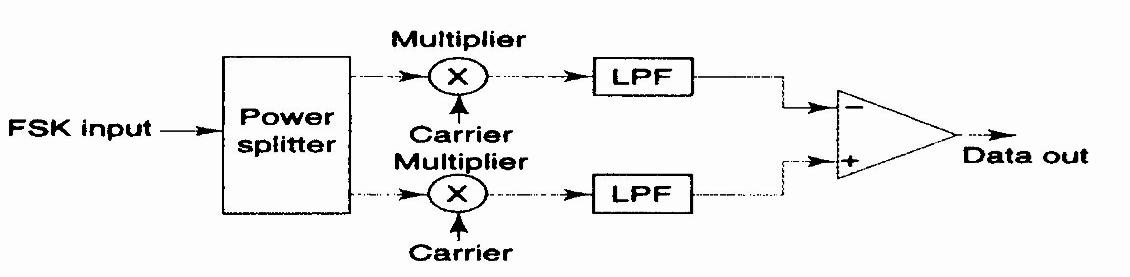
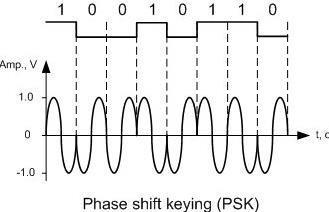


FIGURE 2-8 Coherent FSK demodulator

PHASESHIFT KEYING:

The phase of the output signal gets shifted depending upon the input. These are mainly of two types, namely BPSK and QPSK, according to the number of phase shifts. The other one is DPSK which changes the phase according to the previous value.



Phase Shift Keying (PSK) is the digital modulation technique in which the phase of the carrier signal is changed by varying the sine and cosine inputs at a particular time. PSK technique is widely used for wireless LANs, bio-metric, contactless operations, along with RFID and Bluetooth communications.

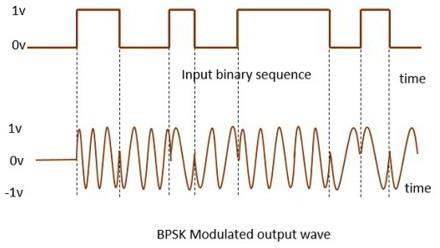
PSK is of two types, depending upon the phases the signal gets shifted. They are −

Binary Phase Shift Keying (BPSK)

This is also called as 2-phase PSK (or) Phase Reversal Keying. In this technique, the sine wave carrier takes two phase reversals such as 0° and 180°.

BPSK is basically a DSB-SC (Double Sideband Suppressed Carrier) modulation scheme, for message being the digital information.

Following is the image of BPSK Modulated output wave along with its input.



Binary Phase-Shift Keying

The simplest form of PSK is *binary phase-shift keying* (BPSK), where N *=* 1 and *M =* *2.*Therefore, with BPSK, two phases (21= 2) are possible for the carrier.One phase represents alogic 1, and the other phase represents a logic 0. As the input digital signal changes state (i.e., from a 1 to a 0 or from a 0 to a 1), the phase of the output carrier shifts between two angles that are separated by 180°.

Hence, other names for BPSK are *phase reversal keying* (PRK) and *biphase modulation.* BPSK is a form of square-wave modulation of a *continuous wave (CW)* signal.

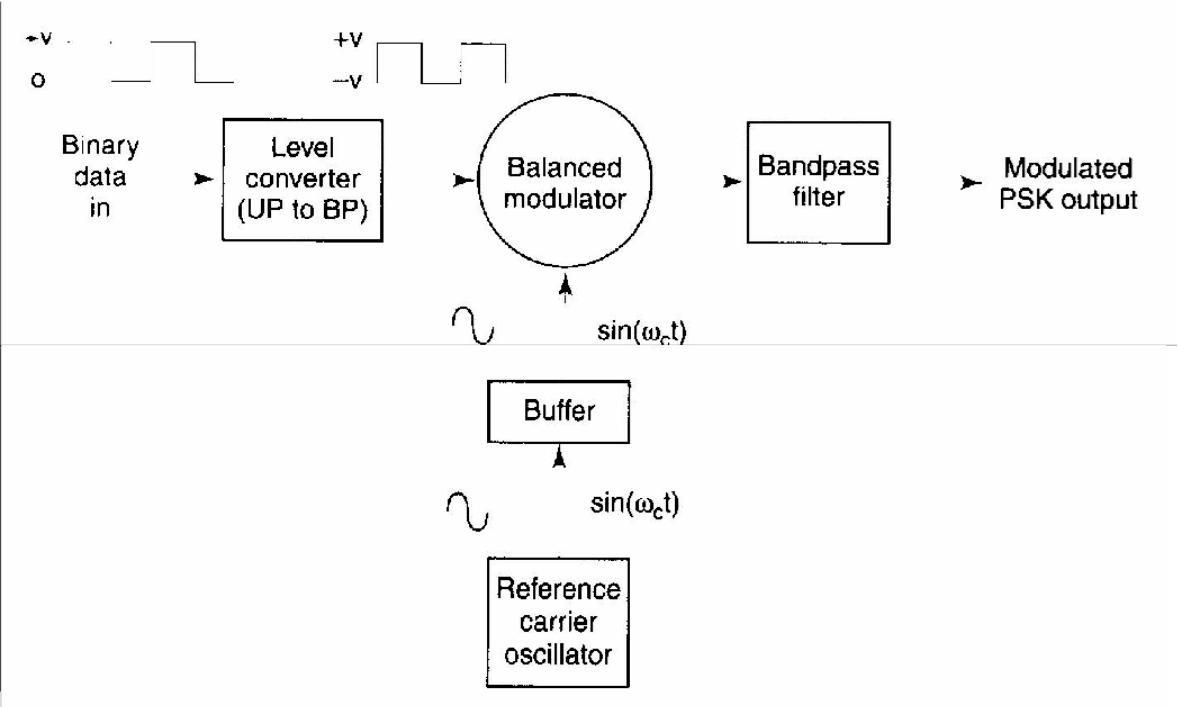


FIGURE 2-12 BPSK transmitter

BPSK TRANSMITTER:

Figure 2-12 shows a simplified block diagram of a BPSK transmitter. The balanced modulator acts as a phase reversing switch. Depending on the logic condition of the digital input, the carrier is transferred to the output either in phase or 180° out of phase with the reference carrier oscillator.

Figure 2-13 shows the schematic diagram of a balanced ring modulator. The balanced modulator has two inputs: a carrier that is in phase with the reference oscillator and the binary digital data. For the balanced modulator to operate properly, the digital input voltage must be much greater than the peak carrier voltage.

This ensures that the digital input controls the on/off state of diodes D1 to D4. If the binary input is a logic 1(positive voltage), diodes D 1 and D2 are forward biased and on, while diodes D3 and D4

are reverse biased and off (Figure 2-13b). With the polarities shown, the carrier voltage is developed across transformer T2 in phase with the carrier voltage across T

1. Consequently, the output signal is in phase with the reference oscillator.

If the binary input is a logic 0 (negative voltage), diodes Dl and D2 are reverse biased and off, while diodes D3 and D4 are forward biased and on (Figure 9-13c). As a result, the carrier voltage is developed across transformer T2 180° out of phase with the carrier voltage across T 1.

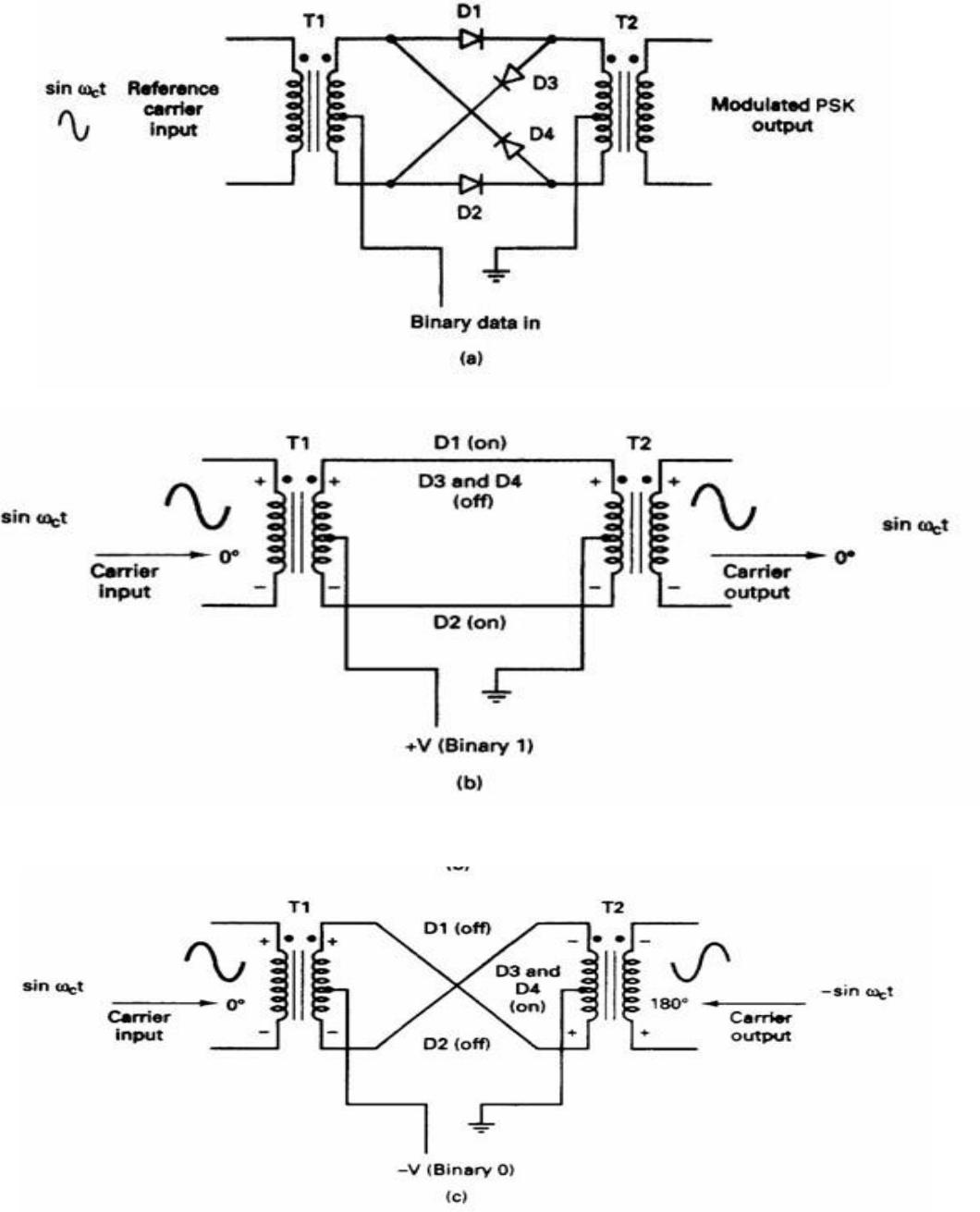
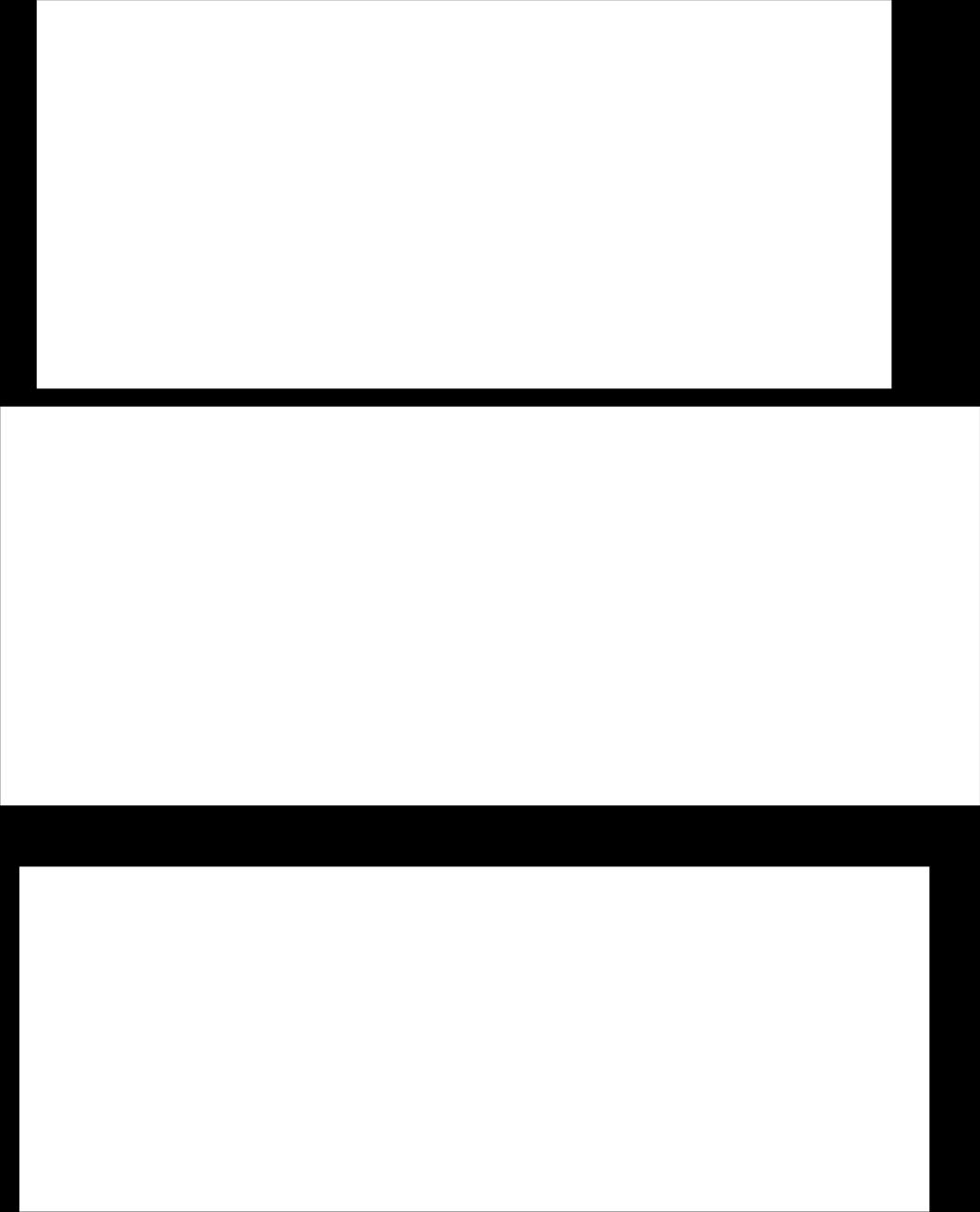


FIGURE 9-13 (a) Balanced ring modulator; (b) logic 1 input; (c) logic 0 input

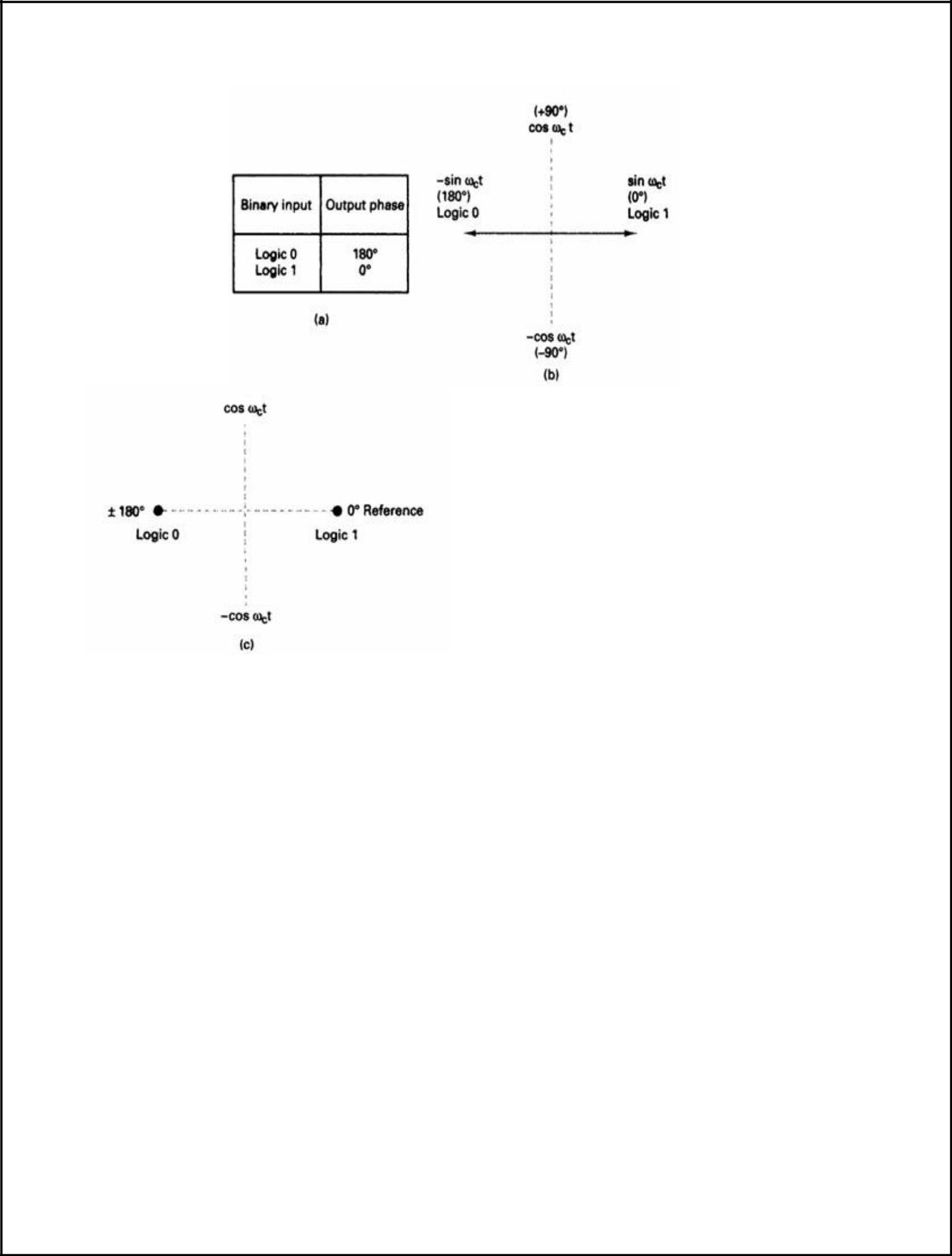


FIGURE 2-14 BPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

BANDWIDTH CONSIDERATIONS OF BPSK:

In a BPSK modulator. the carrier input signal is multiplied by the binary data.

If + 1 V is assigned to a logic 1 and -1 V is assigned to a logic 0, the input carrier (sin ωct) is multiplied by either a + or - 1 .

The output signal is either + 1 sin ωct or -1 sin ωct the first represents a signal that is *in phase* with the reference oscillator, the latter a signal that is 180° out of phase with the reference oscillator.Each time the input logic condition changes, the output phase changes.

Mathematically, the output of a BPSK modulator is proportional to

|  |  |
| --- | --- |
| BPSK output = [sin (2πfat)] x [sin (2πfct)] | (2.20) |

where

fa = maximum fundamental frequency of binary input (hertz)

fc = reference carrier frequency (hertz)

Solving for the trig identity for the product of two sine functions,

0.5cos[2π(fc – fa)t] – 0.5cos[2π(fc + fa)t]

Thus, the minimum double-sided Nyquist bandwidth *(B) is*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| fc + fa |  |  | fc + fa | | | |
| -(fc + fa) | or | -f c + f a | | | | |
|  |  |  |  |  |
|  |  |  |  |  | 2fa | |

and because fa = fb / 2*,* where *fb* *=* input bit rate,

where *B is* the minimum double-sided Nyquist bandwidth.

Figure 2-15 shows the output phase-versus-time relationship for a BPSK waveform. Logic 1 input produces an analog output signal with a 0° phase angle, and a logic 0 input produces an analog output signal with a 180° phase angle.

As the binary input shifts between a logic 1 and a logic 0 condition and vice versa, the phase of the BPSK waveform shifts between 0° and 180°, respectively.

BPSK signaling element *(ts)* is equal to the time of one information bit *(tb),* which indicates that the bit rate equals the baud.

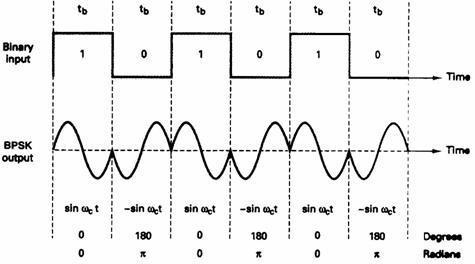


FIGURE 2-15 Output phase-versus-time relationship for a BPSK modulator

Example:

For a BPSK modulator with a carrier frequency of 70 MHz and an input bit rate of 10 Mbps, determine the maximum and minimum upper and lower side frequencies, draw the output spectrum, de-termine the minimum Nyquist bandwidth, and calculate the baud..

Solution

Substituting into Equation 2-20 yields

output = [sin (2πfat)] x [sin (2πfct)]; fa = fb / 2 = 5 MHz

=[sin 2π(5MHz)t)] x [sin 2π(70MHz)t)]

=0.5cos[2π(70MHz – 5MHz)t] – 0.5cos[2π(70MHz + 5MHz)t]

lower side frequency upper side frequency

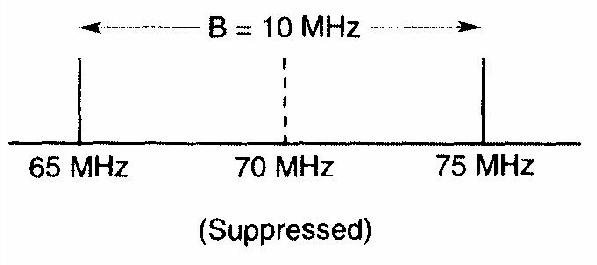
Minimum lower side frequency (LSF):

LSF=70MHz - 5MHz = 65MHz

Maximum upper side frequency (USF):

USF = 70 MHz + 5 MHz = 75 MHz

Therefore, the output spectrum for the worst-case binary input conditions *is* as follows: The minimum Nyquist bandwidth *(B) is*

**

*B* = 75 MHz - 65 MHz = 10 MHz

and the baud *= fb* or 10 megabaud.

BPSK receiver:.

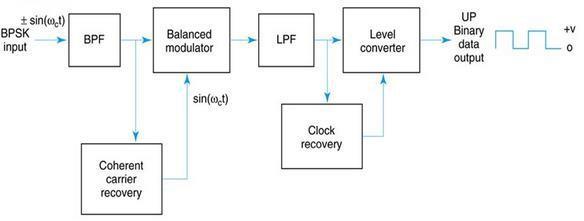
Figure 2-16 shows the block diagram of a BPSK receiver.

The input signal maybe+ sin ωct or - sin ωct .The coherent carrier recovery circuit detects and regenerates a carrier signal that is both frequency and phase coherent with the original transmit carrier.

The balanced modulator is a product detector; the output is the product d the two inputs (the BPSK signal and the recovered carrier).

The low-pass filter (LPF) operates the recovered binary data from the complex demodulated signal.

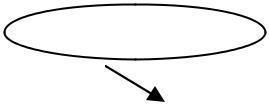
FIGURE 2-16 Block diagram of a BPSK receiver



Mathematically, the demodulation process is as follows.

For a BPSK input signal of + sin ωct (logic 1), the output of the balanced modulator is

|  |  |  |
| --- | --- | --- |
|  | output = (sin ωct )(sin ωct) = sin2ωct | (2.21) |
| or | sin2ωct = 0.5(1 – cos 2ωct) = 0.5 - 0.5cos 2ωct |  |
|  | filtered out |  |



leaving output = + 0.5 V = logic 1

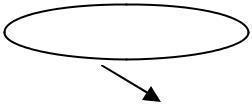
It can be seen that the output of the balanced modulator contains a positive voltage (+[1/2]V) and a cosine wave at twice the carrier frequency (2 ωct ).

The LPF has a cutoff frequency much lower than 2 ωct, and, thus, blocks the second harmonic of the carrier and passes only the positive constant component. A positive voltage represents a demodulated logic 1.

For a BPSK input signal of -sin ωct (logic 0), the output of the balanced modulator is

output = (-sin ωct )(sin ωct) = sin2ωct

or



sin2ωct = -0.5(1 – cos 2ωct) = 0.5 + 0.5cos 2ωct

filtered out

output = - 0.5 V = logic 0

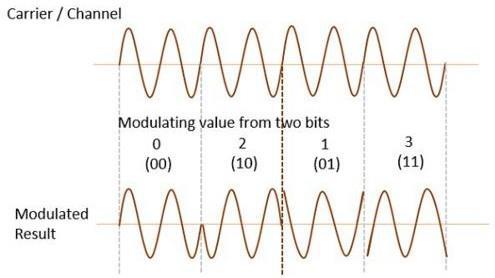
The output of the balanced modulator contains a negative voltage (-[l/2]V) and a cosine wave at twice the carrier frequency (2ωct).

Again, the LPF blocks the second harmonic of the carrier and passes only the negative constant component. A negative voltage represents a demodulated logic 0.

QUADRATURE PHASE SHIFT KEYING (QPSK):

This is the phase shift keying technique, in which the sine wave carrier takes four phase reversals such as 0°, 90°, 180°, and 270°.

If this kind of techniques are further extended, PSK can be done by eight or sixteen values also, depending upon the requirement. The following figure represents the QPSK waveform for two bits input, which shows the modulated result for different instances of binary inputs.



QPSK is a variation of BPSK, and it is also a DSB-SC (Double Sideband Suppressed Carrier)

modulation scheme, which sends two bits of digital information at a time, called as bigits.

Instead of the conversion of digital bits into a series of digital stream, it converts them into bit -pairs.

This decreases the data bit rate to half, which allows space for the other users.

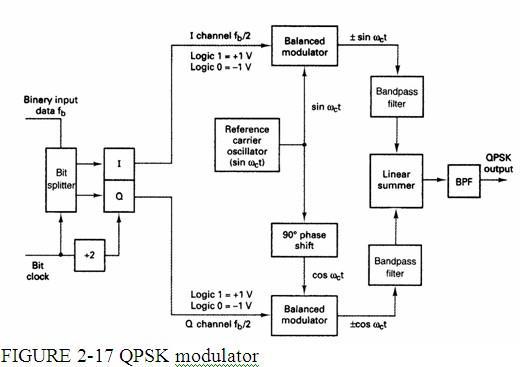
QPSK transmitter.

A block diagram of a QPSK modulator is shown in Figure 2-17Two bits (a dibit) are clocked into the bit splitter. After both bits have been serially inputted, they are simultaneously parallel outputted.

The I bit modulates a carrier that is in phase with the reference oscillator (hence the name "I" for "in phase" channel), and theQ bit modulate, a carrier that is 90° out of phase.

For a logic 1 = + 1 V and a logic 0= - 1 V, two phases are possible at the output of the I balanced modulator (+sin ωct and - sin ωct), and two phases are possible at the output of the Q balanced modulator (+cos ωct), and (-cos ωct).

When the linear summer combines the two quadrature (90° out of phase) signals, there are four possible resultant phasors given by these expressions: + sin ωct + cos ωct, + sin ωct - cos ωct, -sin ωct + cos ωct, and -sin ωct - cos ωct.



Example:

For the QPSK modulator shown in Figure 2-17, construct the truthtable, phasor diagram, and constellation diagram.

Solution

For a binary data input of Q = O and I= 0, the two inputs to the Ibalanced modulator are -1 and sin ωct, and the two inputs to the Q balanced modulator are -1 and cos ωct.

Consequently, the outputs are

I balanced modulator =(-1)(sin ωct) = -1 sin ωct

1. balanced modulator =(-1)(cos ωct) *=* -1 cos ωct and the output of the linear summer is -1 cos ωct - 1 sin ωct = 1.414 sin(ωct - 135°)

For the remaining dibit codes (01, 10, and 11), the procedure is the same. The results are shown in Figure 2-18a.

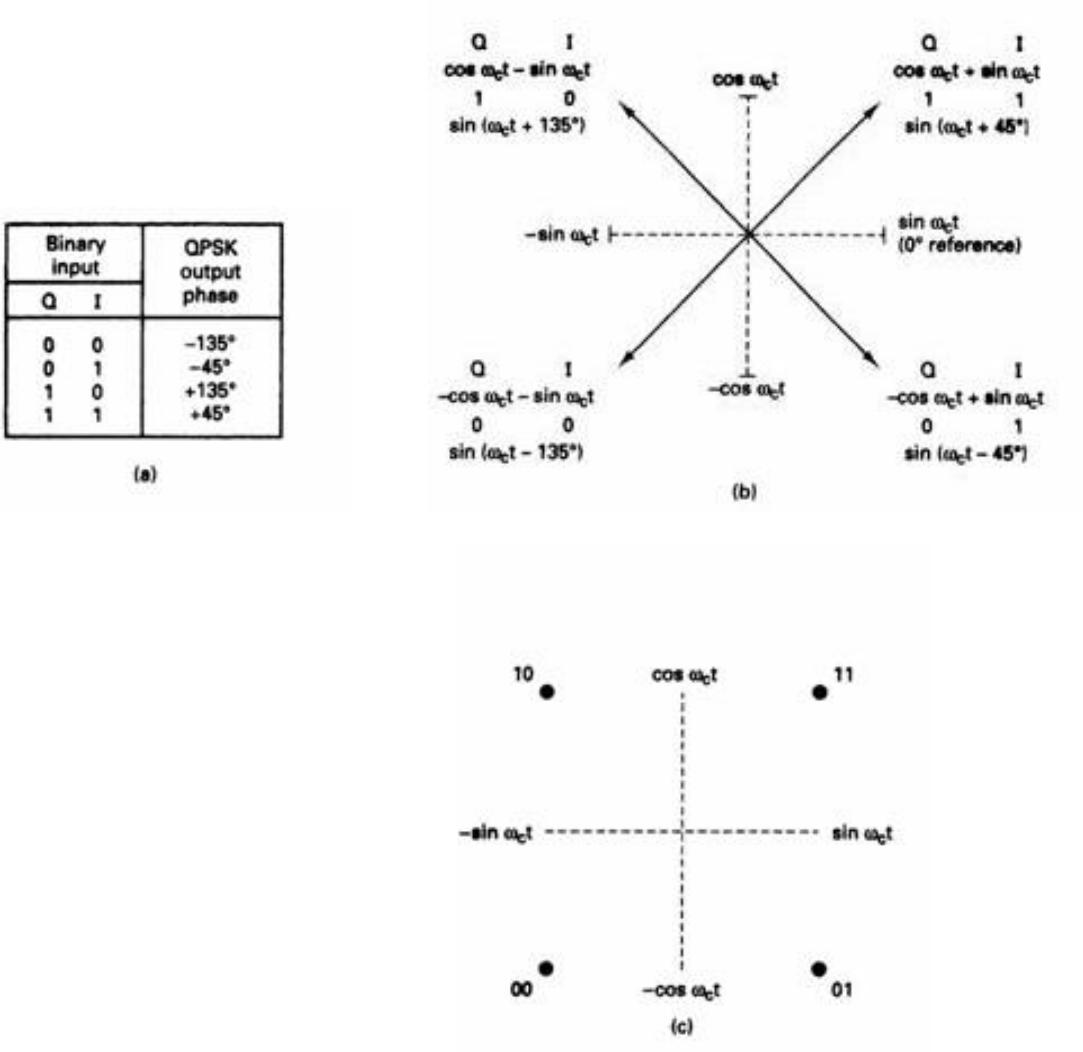
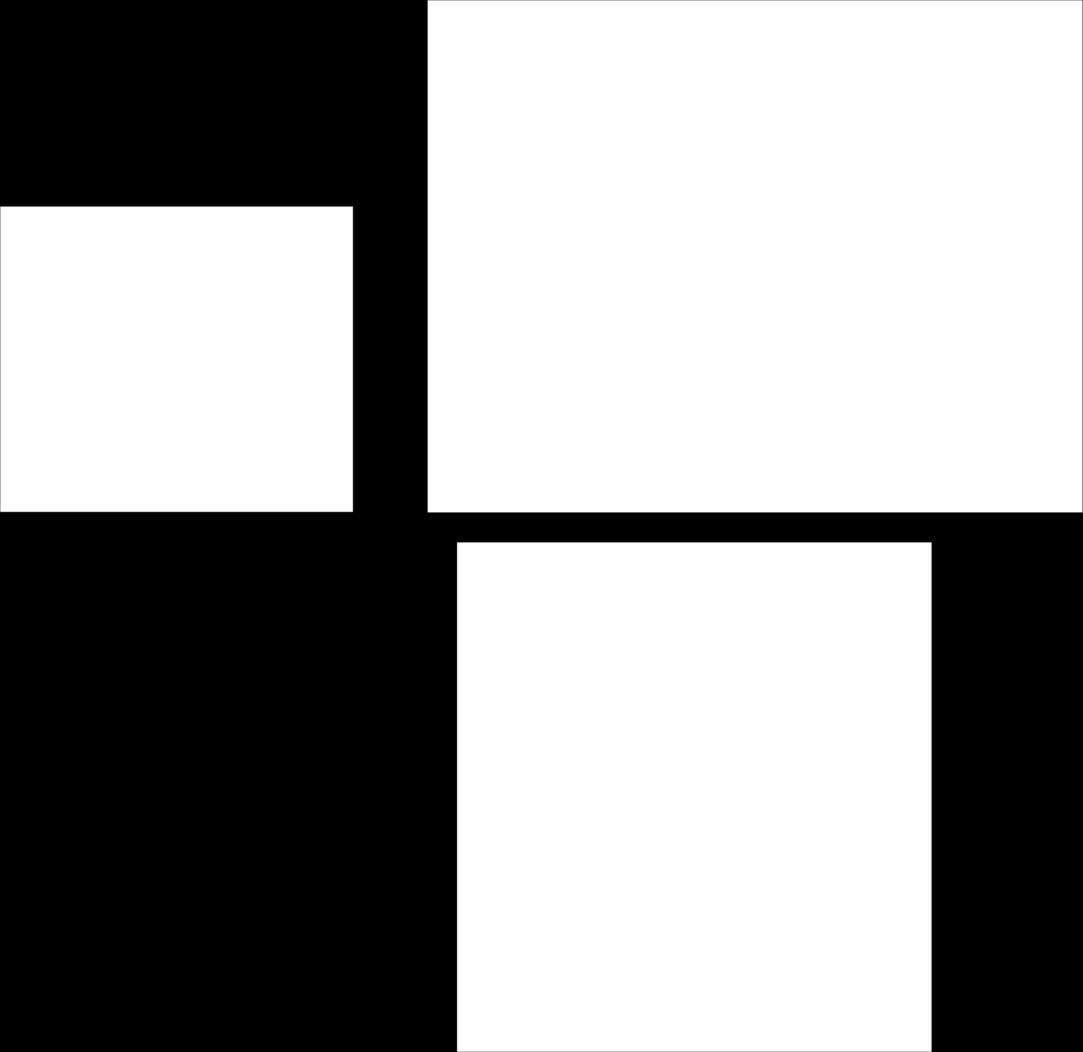


FIGURE 2-18 QPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

In Figures 2-18b and c, it can be seen that with QPSK each of the four possible output phasors has exactly the same amplitude. Therefore, the binary information must be encoded entirely in the phase of the output signal

Figure 2-18b, it can be seen that the angular separation between any two adjacent phasors in QPSK is 90°.Therefore, a QPSK signal can undergo almost a+45° or -45° shift in phase during transmission and still retain the correct encoded information when demodulated at the receiver.

Figure 2-19 shows the output phase-versus-time relationship for a QPSK modulator.

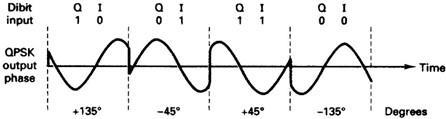
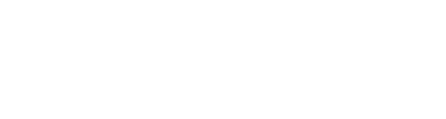


FIGURE 2-19 Output phase-versus-time relationship for a PSK modulator

Bandwidth considerations of QPSK

With QPSK, because the input data are divided into two channels, the bit rate in either the I or the Q channel is equal to one-half of the input data rate (fb/2) (one-half of fb/2 *=* fb/4*).*

QPSK RECEIVER:

The block diagram of a QPSK receiver is shown in Figure 2-21

The power splitter directs the input QPSK signal to the I and Q product detectors and the carrier recovery circuit. The carrier recovery circuit reproduces the original transmit carrier oscillator signal. The recovered carrier must be frequency and phase coherent with the transmit reference carrier. The QPSK signal is demodulated in the I and Q product detectors, which generate the original I and Q data bits. The outputs of the product detectors are fed to the bit combining circuit, where they are converted from parallel I and Q data channels to a single binary output data stream. The incoming QPSK signal may be any one of the four possible output phases shown in Figure 2-

1. To illustrate the demodulation process, let the incoming QPSK signal be -sin ωct + cos ωct. Mathematically, the demodulation process is as follows.

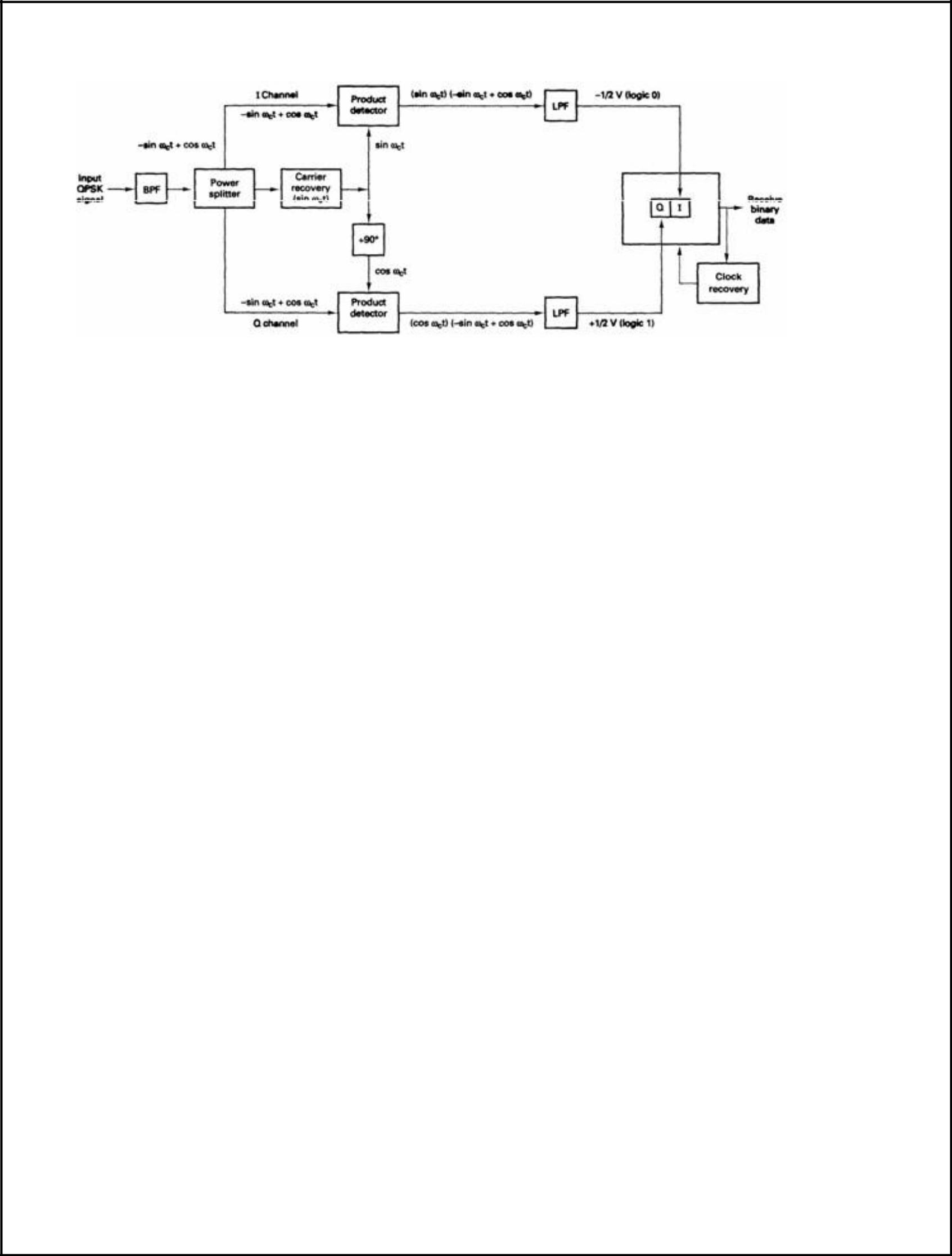
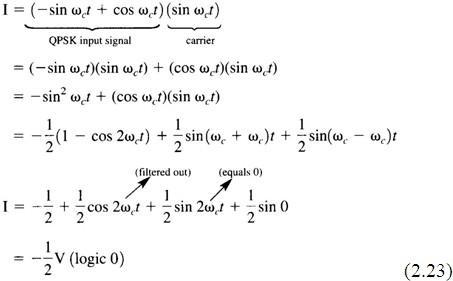
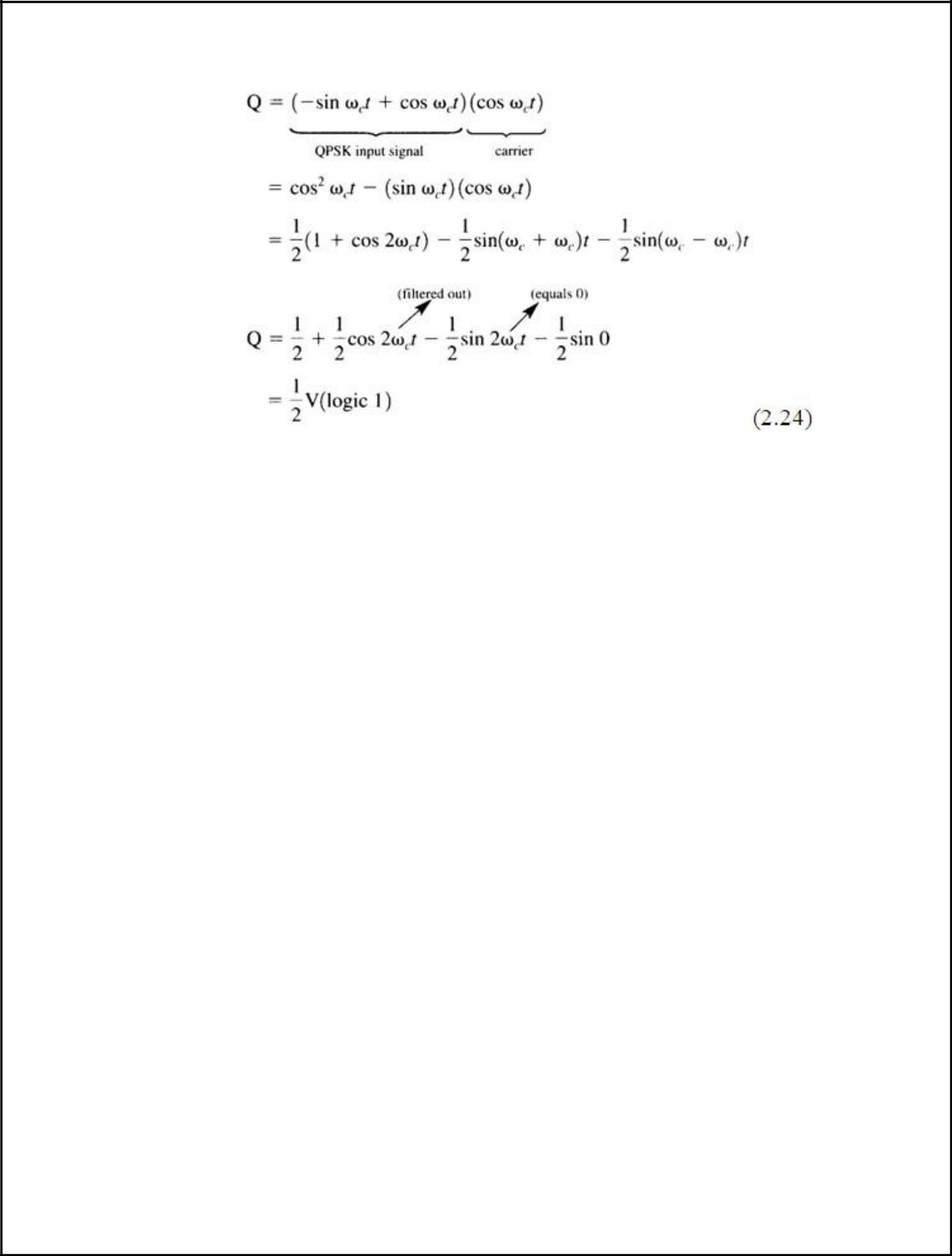


FIGURE 2-21 QPSK receiver

The receive QPSK signal (-sin ωct + cos ωct) is one of the inputs to the I product detector. The other input is the recovered carrier (sin ωct). The output of the I product detector is



Again, the receive QPSK signal (-sin ωct + cos ωct) is one of the inputs to the Q product detector. The other input is the recovered carrier shifted 90° in phase (cos ωct). The output of the Q product detector is

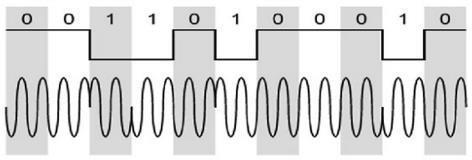


The demodulated I and Q bits (0 and 1, respectively) correspond to the constellation diagram and truth table for the QPSK modulator shown in Figure 2-18.

DIFFERENTIAL PHASE SHIFT KEYING (DPSK):

In DPSK (Differential Phase Shift Keying) the phase of the modulated signal is shifted relative to the previous signal element. No reference signal is considered here. The signal phase follows the high or low state of the previous element. This DPSK technique doesn’t need a reference oscillator.

The following figure represents the model waveform of DPSK.



It is seen from the above figure that, if the data bit is LOW i.e., 0, then the phase of the signal is not

reversed, but is continued as it was. If the data is HIGH i.e., 1, then the phase of the signal is

reversed, as with NRZI, invert on 1 (a form of differential encoding).

If we observe the above waveform, we can say that the HIGH state represents an M in the modulating signal and the LOW state represents a W in the modulating signal.

The word binary represents two-bits. M simply represents a digit that corresponds to the number of conditions, levels, or combinations possible for a given number of binary variables.

This is the type of digital modulation technique used for data transmission in which instead of one-bit, two or more bits are transmitted at a time. As a single signal is used for multiple bit transmission, the channel bandwidth is reduced.

DPSK TRANSMITTER.:

Figure 2-37a shows a simplified block diagram of a *differential binary phase-shift keying* (DBPSK) transmitter. An incoming information bit is XNORed with the preceding bit prior to entering the BPSK modulator (balanced modulator).

For the first data bit, there is no preceding bit with which to compare it. Therefore, an initial reference bit is assumed. Figure 2-37b shows the relationship between the input data, the XNOR output data, and the phase at the output of the balanced modulator. If the initial reference bit is assumed a logic 1, the output from the XNOR circuit is simply the complement of that shown.

In Figure 2-37b, the first data bit is XNORed with the reference bit. If they are the same, the XNOR output is a logic 1; if they are different, the XNOR output is a logic 0. The balanced modulator operates the same as a conventional BPSK modulator; a logic I produces +sin ωct at the output, and A logic 0 produces –sin ωct at the output.

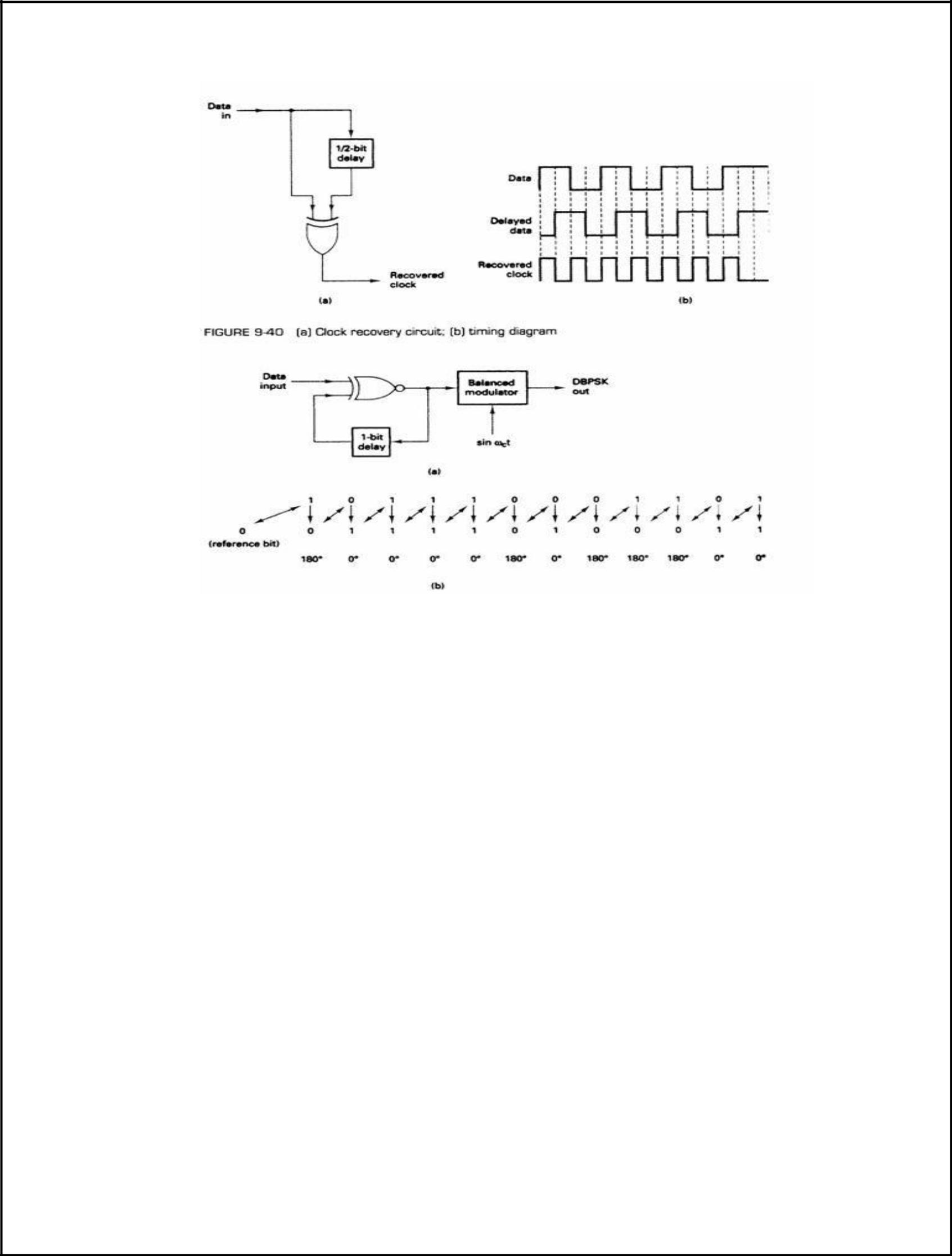


FIGURE 2-37 DBPSK modulator (a) block diagram (b) timing diagram

DPSK RECEIVER:

Figure 9-38 shows the block diagram and timing sequence for a DPSK receiver. The received signal is delayed by one bit time, then compared with the next signaling element in the balanced modulator. If they are the same. J logic 1(+ voltage) is generated. If they are different, a logic 0 (-voltage) is generated. [f the reference phase is incorrectly assumed, only the first demodulated bit is in error. Differential encoding can be implemented with higher-than-binary digital modulation schemes, although the differential algorithms are much more complicated than for DPS K.

The primary advantage of DPSK is the simplicity with which it can be implemented. With DPSK, no carrier recovery circuit is needed. A disadvantage of DPSK is, that it requires between 1 dB and 3 dB more signal-to-noise ratio to achieve the same bit error rate as that of absolute PSK.

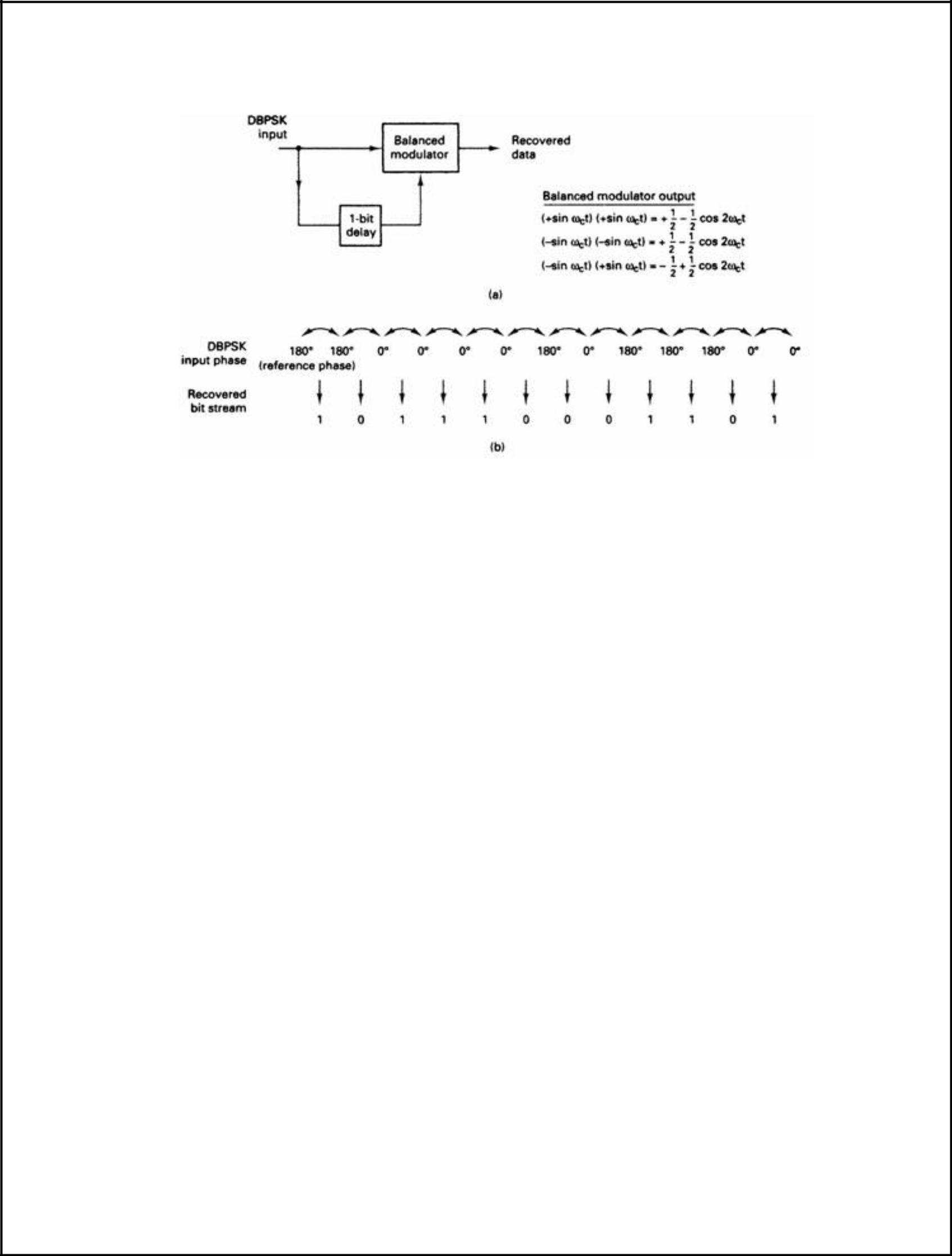


FIGURE 2-38 DPSK demodulator: (a) block diagram; (b) timing sequence

COHERENT RECEPTION OF FSK:

The coherent demodulator for the coherent FSK signal falls in the general form of coherent demodulators described in Appendix B. The demodulator can be implemented with two correlators as shown in Figure 3.5, where the two reference signals are cos(27r f t) and cos(27r fit). They must be synchronized with the received signal. The receiver is optimum in the sense that it minimizes the error probability for equally likely binary signals. Even though the receiver is rigorously derived in Appendix B, some heuristic explanation here may help understand its operation. When s 1 (t) is transmitted, the upper correlator yields a signal 1 with a positive signal component and a noise component. However, the lower correlator output 12, due to the signals' orthogonality, has only a noise component. Thus the output of the summer is most likely above zero, and the threshold detector will most likely produce a 1. When s2(t) is transmitted, opposite things happen to the two correlators and the threshold detector will most likely produce a 0. However, due to the noise nature that its values range from -00 to m, occasionally the noise amplitude might overpower the signal amplitude, and then detection errors will happen. An alternative to Figure 3.5 is to use just one correlator with the reference signal cos (27r f t) - cos(2s f2t) (Figure 3.6). The correlator in Figure

can be replaced by a matched filter that matches cos(27r fit) - cos(27r f2t) (Figure 3.7). All

implementations are equivalent in terms of error performance (see Appendix B). Assuming an AWGN channel, the received signal is



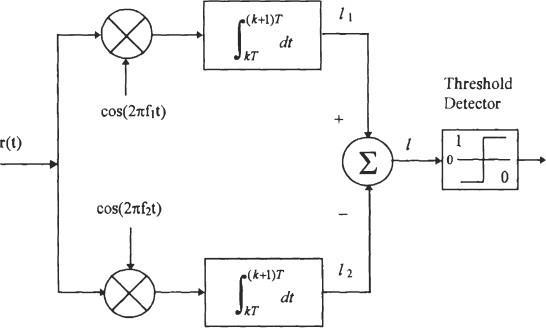
where n(t) is the additive white Gaussian noise with zero mean and a two-sided power spectral density A',/2. From (B.33) the bit error probability for any equally likely binary signals is



where No/2 is the two-sided power spectral density of the additive white Gaussian noise. For Sunde's FSK signals El = Ez = Eb, pI2 = 0 (orthogonal). thus the error probability is



where Eb = A2T/2 is the average bit energy of the FSK signal. The above Pb is plotted in Figure 3.8 where Pb of noncoherently demodulated FSK, whose expression will be given shortly, is also plotted for comparison.



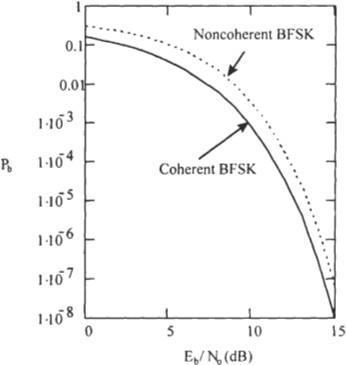


Figure: Pb of coherently and non-coherently demodulated FSK signal.

NONCOHERENT DEMODULATION AND ERROR PERFORMANCE:

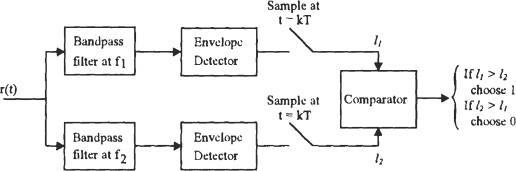
Coherently FSK signals can be noncoherently demodulated to avoid the carrier recovery. Noncoherently generated FSK can only be noncoherently demodulated. We refer to both cases as noncoherent FSK. In both cases the demodulation problem becomes a problem of detecting signals with unknown phases. In Appendix B we have shown that the optimum receiver is a quadrature receiver. It can be implemented using correlators or equivalently, matched filters. Here we assume that the binary noncoherent FSK signals are equally likely and with equal energies. Under these assumptions, the demodulator using correlators is shown in Figure 3.9. Again, like in the coherent case, the optimality of the receiver has been rigorously proved (Appendix B). However, we can easily understand its operation by some heuristic argument as follows. The received signal (ignoring noise for the moment) with an unknown phase can be written as



The signal consists of an in phase component A cos 8 cos 27r f t and a quadrature component A sin 8 sin 2x f,t sin 0. Thus the signal is partially correlated with cos 2s fit and partiah'y correlated with sin 27r fit. Therefore we use two correlators to collect the signal energy in these two parts. The outputs of the in phase and quadrature correlators will be cos 19 and sin 8, respectively. Depending on the value of the unknown phase 8, these two outputs could be anything in (- 5, y). Fortunately the squared sum of these two signals is not dependent on the unknown phase. That is



This quantity is actually the mean value of the statistics I? when signal si (t) is transmitted and noise is taken into consideration. When si (t) is not transmitted the mean value of 1: is 0. The comparator decides which signal is sent by checking these I?. The matched filter equivalence to Figure 3.9 is shown in Figure 3.10 which has the same error performance. For implementation simplicity we can replace the matched filters by bandpass filters centered at f and fi, respectively (Figure 3.1 1). However, if the bandpass filters are not matched to the FSK signals, degradation to



various extents will result. The bit error probability can be derived using the correlator demodulator (Appendix B). Here we further assume that the FSK signals are orthogonal, then from Appendix B the error probability is

