Code No: RT31041 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, May - 2017

PULSE AND DIGITAL CIRCUITS

(Common to Electronics and Communications Engineering, Electronics and Instrumentation Engineering**)**

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) Define Integrator and condition for good integrator circuit. [3M]
b) Design a 2-different positive level clipper circuit. [4M]
c) Define 'ON' time and 'OFF' time of a transistor in terms of transistor switching times? [3M]
d) Define the types of states in multi vibrators. [3M]
e) Define the slope or sweep-speed error. [3M]
f) Define Pedastal height. [3M]
g) Explain the need of commutating capacitor in bistable multivibrator. [3M]

PART –B

2 a) Prove that e_t = T/2RC for ramp as input to the High pass RC-Circuit? [6M]
b) Explain the working principle of rate-of-rise amplifier? [5M]
c) Explain the working of attenuator as a CRO Probe? [5M]

3 a) Prove that external resistance $R=\sqrt{R_r \times R_f}$ in a clipping circuit? [6M]
b) Discuss the function of series diode and shunt diode clipping circuits? How can the clipping level shifted to reference voltage? Explain? [10M]

4 a) Explain the breakdown voltage consideration of a transistor. [5M]
b) Design and explain 2-input ECL OR/NOR gate. [6M]
c) Define voltage levels and noise margin of 10KECL family. [5M]

5 a) Derive the equation for voltage-to-frequency converter when a stable multi vibrator is used as a basic circuit. [8M]
b) The Schmitt trigger circuit also called sinusoidal to square converter? Explain the working principle. [8M]

6 a) Explain the working principle of UJT sweep circuit. [8M]
b) Explain the working principle of Boot-strap –time base generator. [8M]

7 a) Draw and explain the reduction of pedestal techniques in a gate circuit. [8M]
b) Explain, how monostable multivibrator can be used for frequency division? [8M]

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Code No: RT22023 **R13** SET - 1

II B. Tech II Semester Regular/Supplementary Examinations, April/May-2017
PULSE AND DIGITAL CIRCUITS
(Com. to EEE, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Write the application of attenuator (4M)
   b) State the clamping theorem (3M)
   c) Write the application of Monostable multi vibrator (3M)
   d) Draw the diagram for Diode two input AND gate (4M)
   e) Define the terms i) voltage time base generator ii) current time base generator (4M)
   f) What are the advantages and disadvantages of unidirectional diode gate (4M)

PART –B

2. a) Derive an expression for the upper cut-off frequency of low pass RC circuit (8M)
   b) A symmetrical square wave whose peak-to-peak amplitude is 2V and whose average value is zero as applied to on RC integrating circuit. The time constant is equals to half -period of the square wave? find the peak to peak value of the output amplitude (8M)

3. a) Explain how a sine wave may be converted into a square wave using a clipping circuit (8M)
   b) T=1000 μ sec (8M)
   V= 10 V
   Duty cycle = 0.2
   i) Sketch waveform with voltage levels at steady state Figure 1.
   ii) Forward and reverse direction tilt
   iii) Af/ Ar

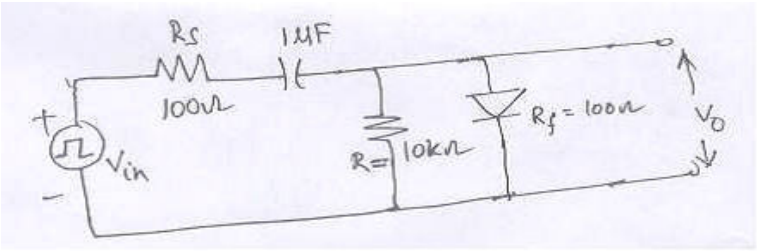

Figure 1

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4. a) Derive an expression for the gate width of a mono-stable multivibrator (8M)
   b) A collector coupled Fixed bias binary uses NPN transistors with h_{FE}= 100. The circuit parameters are VCC = 12v, VBB = -3v, RC = 1k , R1 = 5k , and R2 = 10 k. Verify that when one transistor is cut-off the other is in saturation. Find the stable state currents and voltages for the circuit. Assume for transistors VCE(sat) = 0.3V and VBE(sat) = 0.7V (8M)

5. a) What is positive and negative logic system (8M)
   b) With the help of a neat circuit diagram for NOR gate using ECL logic and explain. (8M)

6. a) Explain with neat diagram and working of a UJT time base generator (8M)
   b) Explain the basic principles of the Miller and bootstrap time base generator (8M)

7. a) How does the synch signal affect the frequency of operation of the sweep generator? (8M)
   b) Explain use of a mono stable relaxation device as a divider (8M)

Code No: RT22023 **R13** SET - 2

II B. Tech II Semester Regular/Supplementary Examinations, April/May-2017
PULSE AND DIGITAL CIRCUITS
(Com. to EEE, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) What do you mean by (i) over compensation (ii) under compensation (4M)
   b) What is the difference between clipping and clamping (4M)
   c) What are the applications of Schmitt trigger? (3M)
   d) Draw the diagram for Diode two input OR gate (4M)
   e) Draw the sweep waveform and define the parts of the waveform? (4M)
   f) What are the advantages with diode sampling gate (3M)

PART -B

2. a) Derive an expression for the rise time of the output of a low pass circuit excited by a step input (8M)
   b) Three low pass RC circuits are in cascade and isolated from one another by ideal buffer amplifiers. Find the expression for the output voltage as a function of time if the input is a step voltage. (8M)

3. a) With the help of a neat circuit diagram, explain the working of an emitter-coupled clipper (8M)
   b) The input voltage vi to the two level clipper shown in Figure 1, varies linearly from 0 to 75 V. Sketch the output voltage vo to the same time scale as the input voltage. Assume Ideal diodes. (8M)

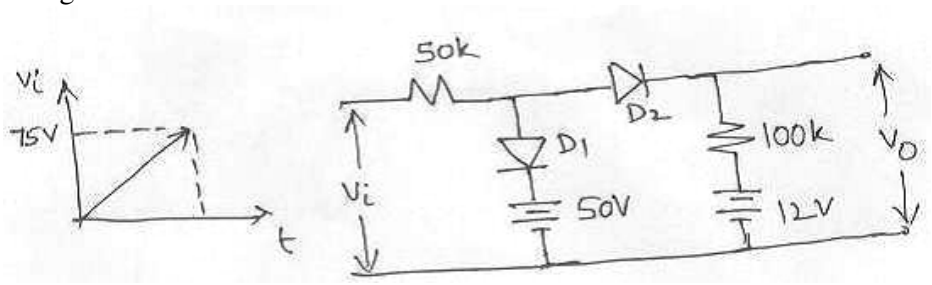

Figure 1

4. a) Derive an expression for the UTP and LTP of Schmitt trigger. (8M)
   b) Design a collector coupled transistor monostable multivibrator to produce a time delay of 100 μ sec. Use transistors have h_{FE} of 250. Use ±12 v sources, $V_{CE}(sat)$ = 0.3 v, $V_{BE}(sat)$ = 0.7 v and V_{BE} cutoff = 0v. (8M)
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5. a) Explain with suitable diagram of 3-input AND gate TTL? (8M)
   b) With the help of a neat circuit diagram for NAND gate using ECL logic and explain. (8M)

6. a) Define below terms and derive the relation between (8M)
      i) sweep speed error
      ii) displacement error
      iii) transmission error
   b) Explain in detail the working of a transistor Miller time-base generator (8M)

7. a) Explain in detail frequency division by an astable blocking oscillator (8M)
   b) Explain the synchronization of a sweep circuit with symmetrical signals (8M)

Code No: RT22023 **R13** SET - 3

II B. Tech II Semester Regular/Supplementary Examinations, April/May-2017
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Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) If IV is the peak to peak of differentiator? What is the output of peak to peak? (4M)
   b) What is shunt noise clipper (3M)
   c) What is a non-saturated binary? Write its advantages and disadvantages (3M)
   d) Write the advantages and disadvantages of TTL family (4M)
   e) Define flyback time and sweep time? (4M)
   f) What are the drawbacks of two diode gates? (4M)

PART -B

2. a) Derive an expression for the output of a high-pass circuit excited by a ramp input (8M)
   b) Sketch the output waveform for square wave input. A pulse of 5 v amplitude and pulse width 0.5 m sec is applied to high pass RC circuit consisting of R = 22 kΩ and C = 0.47 μf. Determine the % tilt in the output waveform. (8M)

3. a) Design a diode clamper to restore a d.c level of +3 Volts to an input sinusoidal signal of peak value 10Volts. Assume drop across diode is 0.6 volts as shown in the Figure 1. (8M)

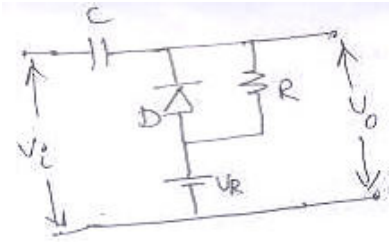

Figure 1

   b) Compare and explain series diode clipper and shunt diode clipper. (8M)

4. What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a Astable multivibrator, and derive an expression for pulse width. Draw the wave forms at collector and Bases of both transistors. (16M)

5. a) Define positive and negative logic system (8M)
   b) With the help of a neat circuit diagram for NAND gate using NMOS logic and explain. (8M)

6. a) Explain various methods of generating time- base waveforms (8M)
   b) Explain general considerations of bootstrap time base generator (8M)

7. a) Explain synchronization of a sweep generator with pulse signals (8M)
   b) Explain use of a mono stable relaxation device as a divider (8M)
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Code No: RT22023 **R13** SET - 4

II B. Tech II Semester Regular/Supplementary Examinations, April/May-2017
PULSE AND DIGITAL CIRCUITS
(Com. to EEE, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Draw the circuit of double differentiator (4M)
   b) What is series noise clipper (3M)
   c) Write the difference between saturated and non-saturated binary (4M)
   d) Write the advantages and disadvantages of DTL family (4M)
   e) What are the applications of time base generator (3M)
   f) What is basic operating principles of sampling gates (4M)

PART –B

2. a) Derive the condition for perfect compensator of an attenuator (8M)
   b) Derive the expression for percentage till for a square wave output of RC high pass circuit. (8M)

3. a) State and prove the clamping circuit theorem (8M)
   b) Determine Vo for the network shown in Figure 1, for the given waveform Assume ideal diodes. (8M)

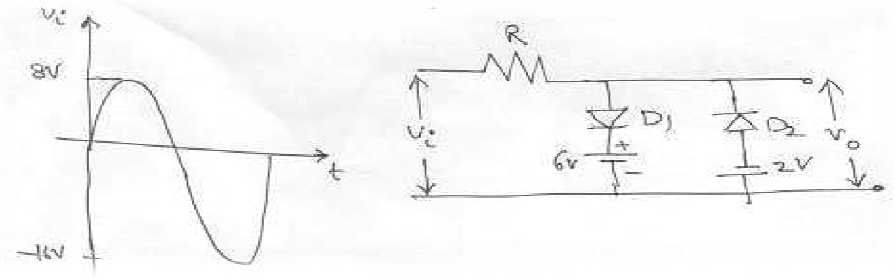

Figure 1

4. With neat diagram explain how to control hysteresis in Schmitt trigger? (16M)

5. a) Explain in detail about CMOS logic-analysis (8M)
   b) With the help of a neat circuit diagram for NAND gate using PMOS logic and explain. (8M)

6. a) Explain in detail about transistor constant current sweep (8M)
   b) Explain the effect of gate width w.r. to voltage in boot strap circuit (8M)

7. a) What is the condition to met for pulse synchronization of mono-stable circuits (8M)
   b) With the help of neat waveforms, explain sine wave frequency division with a sweep circuit (8M)
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Code No: RT31041 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, May - 2016
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Describe about ringing circuit.	[3M]
	b)	State clamping circuit theorem.	[4M]
	c)	Explain piecewise linear characteristics of a diode.	[4M]
	d)	What are the types of triggering? Distinguish between them.	[4M]
	e)	What are the applications of Time-base generator?	[3M]
	f)	What do you mean by sampling gate? Give the applications of sampling gate?	[4M]

PART -B

2	a)	Discuss about attenuators.	[4M]
	b)	Analyze the low pass circuit for the exponential inputs, with help of waveforms.	[8M]
	c)	Discuss the application of an attenuator in a CRO.	[4M]
3	a)	Draw the basic circuit diagram of positive peak clamper circuit and explain its operation.	[8M]
	b)	Explain transfer characteristics of emitter coupled clipper and derive necessary equations.	[8M]
4	a)	Draw the circuits of 3-input OR-gate using diodes for: (i) Positive logic, (ii) Negative logic and explain the operation of circuit.	[8M]
	b)	Give the comparison of different logic families.	[8M]
5	a)	What are different types of multivibrators? Explain the stable state of a multivibrator.	[8M]
	b)	Sketch the circuit diagram of Schmitt trigger and explain its operation.	[8M]
6	a)	With the help of neat circuit diagram and waveforms explain transistor miller time base generator.	[8M]
	b)	Discuss about the recovery time of a sweep circuit. How do you achieve short recovery time?	[8M]
7	a)	Explain the process of synchronization of a sweep circuit.	[8M]
	b)	Write notes on: i) Astable relaxation circuits ii) Monostable relaxation circuits	[8M]

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Code No: RT31041 **R13** SET - 1

III B. Tech I Semester Regular Examinations, November- 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	Define storage time and transition time of a diode.	[3M]
	b)	What are the advantages and disadvantages of a direct coupled binary?	[4M]
	c)	What do you mean by phase jitter?	[3M]
	d)	State and prove clamping circuit theorem.	[4M]
	e)	What do you mean by Schotty TTL? Why is it faster than standard TTL?	[4M]
	f)	What does the display of a sampling scope consists of?	[4M]

PART -B

2	a)	Prove that a low pass circuit acts as an integrator. Derive an expression for the output voltage levels under steady state conditions of a low pass circuit excited by a ramp input.	[8M]
	b)	Explain RLC ringing circuit with a neat sketch.	[8M]
3	a)	Define i) Rise time ii) Fall time iii) Delay time iv) Storage time Explain the factors which contribute to the delay time of transistor.	[8M]
	b)	Draw the circuit of CMOS NOR gate and explain its operation. Mention the advantages of CMOS over the other digital logic families.	[8M]
4	a)	Describe the sequence of events in an n-p-n transistor to change from cutoff to saturation and vice versa. How does temperature affect the saturation junction of a transistor?	[8M]
	b)	Draw and explain the circuit diagram of integrated positive TTL AND & OR gates.	[8M]
5	a)	Explain the operation of a Monostable multivibrator and derive for the pulse width with necessary waveforms & circuirts.	[8M]
	b)	Design a collector coupled astable multivibrator using NPN silicon transistors with h_{fe}=40, r_{bb}=200Ω supploied with Vcc=10V and circuit component values are Rc=1.2KΩ and C=270 pF.	[8M]
6	a)	Explain the working of a transistor Bootstrap sweep circuit and derive expression for the slope sweep error.	[8M]
	b)	Why the time base generators are called sweep circuits? Give most important applications of time –base generators.	[8M]
7	a)	Explain how the loading of the control signal is reduced when the number of inputs increases in a sampling gate.	[8M]
	b)	Draw and explain the waveforms of a frequency division by an Astable multivibrator.	[8M]

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Code No: RT31041 **R13** SET - 2

III B. Tech I Semester Regular Examinations, November - 2015
PULSE AND DIGITAL CIRCUITS
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Time: 3 hours Max. Marks: 70

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2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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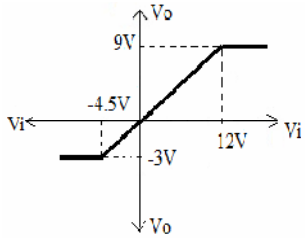
PART –A

1	a)	What are the reasons for existence of rise time and fall time?	[4M]
	b)	Why a monostable multivibrator is also called a delay circuit? Explain.	[3M]
	c)	What do you mean by synchronization on a one-to-one basis and that with frequency division?	[4M]
	d)	Which logic gates are suitable for wired OR operations and why?	[3M]
	e)	What do you mean by pedestal? What are the advantages of diode sampling gates?	[4M]
	f)	What is hysteresis how it can be eliminated in a Schmitt trigger?	[4M]

PART -B

2	a)	Draw the output waveform of an RC high-pass circuit with a square wave input under different time constants. Derive the expression for percentage of tilt.	[8M]
	b)	Draw a Schmitt Trigger using transistors and derive for UTP & LTP.	[8M]
3	a)	Give the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics	[8M]
	b)	State and prove clamping circuit theorem.	[4M]
	c)	The ideal transfer characteristic of particular clipper circuit is shown in Figure.2. Design the circuit using ideal diodes and draw the input-output waveforms with proper explanation, if Vi = 15 Sin ωt.	[4M]



4	a)	Explain with the help of suitable waveforms the switching times of a diode switch. Derive the expression for reverse recovery time.	[8M]
	b)	Draw and explain the circuit diagram of integrated positive RTL NOR gate.	[6M]
	c)	Explain the reason for delay transition in a transistor as a switching element.	[2M]
5	a)	Design and draw a collector-coupled ONE-SHOT using silicon npn transistors with $h_{FE(min)}$ =20. In stable state, the transistor in cut-off has V_{BE} = -1V and the transistor in saturation has base current, I_B which is 50% excess of the $I_{B(min)}$ value. Assume VCC = 8V, IC(sat) =2mA, delay time = 2.5ms & $R_1 = R_2$. Find R_C, R, R1, C and V_{BB} .	[8M]

b) Draw the circuit diagram of an astable multivibrator and obtain all the steady state voltages and currents. Show how it acts as a voltage to frequency converter. [8M]

6 a) What are the different methods of generating time-base waveforms? Explain about each briefly. [8M]

b) Explain the working of Transistor Miller sweep circuit. What are its advantages over Bootstrap sweep circuits? [8M]

7 a) With the help of a neat circuit diagram and waveforms, explain the method to achieve frequency synchronization using pulse train as sync signals. [8M]

b) Explain the function of a sampling gate used in Sampling Scopes also explain how sampling gate is used in chopping amplifiers. [8M]

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Code No: RT31041 **R13** SET - 3

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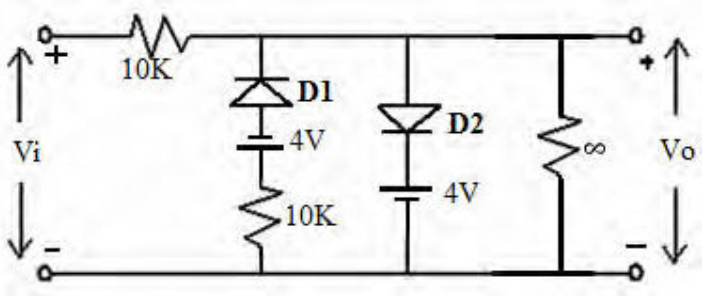
PART –A

1	a)	What is direct coupled binary? Give its advantages and disadvantages.	[4M]
	b)	What do you mean by blocked condition in astable multivibrator?	[3M]
	c)	How is the deviation from linearity expressed?	[3M]
	d)	What do you mean by synchronization? When do we say two waveform generators are synchronized?	[4M]
	e)	What are the advantages of MOS families over bipolar families?	[4M]
	f)	What are the advantages and disadvantages of unidirectional diode gates?	[4M]

PART -B

2	a)	Derive an expression for the output of low pass RC circuit excited by a step input. Draw the output for different time constants.	[8M]
	b)	What is an attenuator? How can an uncompensated attenuator be modified as a compensated attenuator. Give the comparison between perfect compensation, under compensation and over compensation.	[8M]
3	a)	Explain the working of a two-level diode clipper with the help of circuit diagram, waveform and transfer characteristics.	[6M]
	b)	Determine the output waveform for the biased clipping circuit for the square wave input.	[6M]
	c)	A voltage signal of (10 Sinωt) is applied to the circuit with ideal diodes shown in figure below. Estimate the maximum & minimum values of output waveform and maximum current through each diode. Also draw the input-output waveforms with proper explanation	[4M]



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4 a) Briefly discuss the influence of breakdown voltages on the choice of supply voltage in a transistor switch. [4M]

b) Explain the characteristics and implementation of the following digital logic family i) CMOS, ii) ECL [8M]

c) Classify the basic families that belong to the bipolar families and to the MOS families. [4M]

5 a) b) Design a Schmitt trigger circuit using npn silicon transistors with V_{BE} = 0.7V, $V_{CE}(sat)$ = 0.2V, $h_{fe}(min)$ = 60 and $I_C(ON)$ = 3mA to meet the following specifications: V_{CC} =12V, upper threshold voltage, V_{UT} = 4V, lower threshold voltage, V_{LT} =2V. [8M]

b) What are transpose capacitors? Explain how the commutating capacitors will increase the speed of a fixed-bias binary. [8M]

6 a) Define and derive the terms slope error, displacement error and transmission error. [8M]

b) Explain the basic principles of Miller and Bootstrap time-base generators. Give the comparison of both the generation methods. [8M]

7 a) What is synchronization? Why it is necessary in waveform generators? Explain the synchronization of a sweep circuit with symmetrical signals. [8M]

b) Explain how to cancel the pedestal in a sampling gate with suitable circuit diagram. [8M]

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Code No: RT31041 **R13** SET - 4

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2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
*****

PART –A

1	a)	Which signal can preserve its wave shape when transmitted through a linear network and explain how it can.	[4M]
	b)	Show the relationship between the percentage of tilt and cutoff frequency for a high pass RC circuit.	[3M]
	c)	What are the applications of time base generators?	[3M]
	d)	What is non-saturated binary? What are its drawbacks?	[4M]
	e)	What are the merits and demerits of TTL?	[4M]
	f)	Why sampling gates called linear gates and how do they differ from logic gates?	[4M]

PART -B

2	a)	An RC low-pass filter is fed with a symmetrical square wave. The peak-to-peak amplitude of the input waveform is 10 V and its average value is zero. It is given that RC=*T/2* where *T* is the period of the square wave. Determine the peak-to-peak amplitude of the output waveform.	[8M]
	b)	Draw the response of an RC high pass circuit when applied with exponential input. Explain the response for different time constants.	[8M]
3	a)	Draw the circuit diagram and explain the working of transistor clippers.	[6M]
	b)	Draw the basic circuit diagram of negative peak clamper circuit and explain its operation	[7M]
	c)	Give some applications of clipping & Clamping circuits.	[3M]
4	a)	Describe how a transistor functions as a switch in the CE configuration in ON state and in OFF state. How does the temperature affect the saturation junction voltages of a transistor?	[8M]
	b)	Classify the basic families that belong to the bipolar families and to the MOS families.	[4M]
	c)	What is the major difference between TTL and ECL? Why does the propagation delay occur in logic circuits?	[4M]

5 a) A self-biased binary uses n-p-n transistors have maximum values of V_{CE}(sat)=0.4V and V_{BE}(sat) = 0.8V and V_{BE} (cutoff) = 0V. The circuit parameters are V_{CC} = 15V, RC = 1KΩ, R1 = 6KΩ, R2 = 15KΩ and RE = 500Ω. i) Find the stable-state currents and voltages. ii) Find the minimum value of hFE required for BJT to provide the above stable state values. iii) Also determine I_{CBO}(max) to which I_{CBO} raises as temperature rises where neither BJT is off. [8M]

b) Explain various methods to improve the resolution of a binary. [4M]

c) Draw the circuit of a Schmitt trigger and give some of its applications. [4M]

6 a) Explain the basic principle of a bootstrap sweep generator. Draw the circuit and explain its operation. Derive the expression for its slope error. [8M]

b) How is deviation of linearity expressed? What do you mean by sweep time and restoration time? [8M]

7 a) What is meant by synchronization with frequency division? Explain, with suitable waveforms, the procedure to obtain 3:1 and 5:1 synchronization. [8M]

b) Draw the circuit diagram of a unidirectional sampling gate which delivers an output only at the coincidence of a number of control voltages and explain its working. [8M]

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