Code No: RT32042 **R13** SET - 1

III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1 a) Find the power of the given signal below? [4M]

$$x[n] = \begin{cases} 3(-1)^n, & n \geq 0 \\ 0 & n < 0 \end{cases}$$

b) Compare overlap-add method and overlap-save method [4M]

c) Compare direct form I and direct form II realization of IIR systems. [4M]

d) What conditions are to be satisfied by the impulse response of an FIR system in order to have a linear phase? [3M]

e) What is the need for multirate signal processing? [3M]

f) What are the differences between fixed type processors and floating type processors? [4M]

PART –B

2 a) Find the solution to the following linear constant coefficient difference equation [10M]

$$y(n) - \frac{3}{2}\, y\,(n-1) + \frac{1}{2} y(n-2) = \left(\frac{1}{2}\right)^n \; for \; n \geq \; 0$$

With initial conditions y(-1) = 4 and y(-2) = 10.

b) Derive the relationship between impulse response and frequency response of a discrete time system. [6M]

3 a) Compute the DFT of the sequence x(n) = sin[nπ/4], where N=8 using DIT FFT algorithm [8M]

b) Determine the IDFT of the sequence [8M]

$$X(K) = (6, -\sqrt{2} - j4.8284, -2 + j2, \sqrt{2} - j0.8284, -2, \sqrt{2} + j0.8284, -2 - j2, -\sqrt{2} - j4.8284$$

4 Obtain the cascade and parallel realisation structures for the following signals. [16M]

$$H(z) = \frac{2(1 - z^{-1})(1 + \sqrt{2}z^{-1} + z^{-2})}{(1 + 0.5z^{-1}(1 - 0.9z^{-1} + 0.81z^{-2}))}$$

||''|'''|''|'|''''||

5 a) The desired frequency response of a low pass filter is

$$H_d(e^{jw}) = \begin{cases} e^{-j3w} & \frac{-3\pi}{4} \le w \le \frac{3\pi}{4} \\ 0 & elsewhere \end{cases}$$ [10M]

Determine $H(e^{jw})$ for M =7 using a rectangular window.

b) What are the effects of windowing? [6M]

6 a) Derive an expression for the spectrum of output signal of an decimator. [8M]

b) What are the applications of multirate system? [8M]

7 a) What is MAC? Explain its operation in detail. [10M]

b) What are the various addressing modes used in the TMS320C5X processor? [6M]

*****

Code No: RT32042 **R13** SET - 2

III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1 a) Show that the following systems are nonlinear and time invariant. [4M]
$y(n) – x(n)y(n-1) = x(n)$

b) Write computation efficiency of FFT over DFT. [3M]

c) What are the basic building blocks of realization structures? [4M]

d) Obtain the mapping formula for the impulse invariant transformation. [4M]

e) Write some examples of multirate digital systems. [3M]

f) What are the advantages of DSP processors in relation to general purpose processors? [4M]

PART –B

2 a) Determine the frequency response, magnitude and phase responses and time delay of the systems given by [10M]

$$y(n) - \frac{1}{2}y(n-1) = x(n)$$

b) Explain causality and stability of a linear time invariant system. [6M]

3 a) Find the DFT of the following sequence using FFT DIF? [8M]
X(n) = {1,2,3,5,5,3,2,1}

b) Compute the DFTs of the sequence $x(n) = 2^{-n}$, where N = 8 using DIT algorithm [8M]

4 Develop the cascade and parallel forms of the following causal IIR transfer functions. [16M]

$$H(z) = \frac{(3 + 5z^{-1})(0.6 + 3z^{-1})}{(1 - 2z^{-1} + 2z^{-2})(1 - z^{-1})}$$

5 a) Convert the analog filter to a digital filter whose system function is [10M]

$$H(s) = \frac{1}{(s+2)^2 + (s+1)}$$

Use bilinear transformation.

b) What is a Kaiser window? In what way is it superior to other window functions? [6M]

||''|''|''|''|''||

6 a) Draw the block diagram of a multistage interpolator and explain it [8M]

b) A one stage decimator is characterized by the following Decimator factor = 3. Anti-aliasing filter coefficients h(0) = -0.06 = h(4), h(1)=0.3 =h(3), h(2) =0.62. Given the data, s(n) with successive values [6,-2,-3,8,6,4,-2], calculate and list the filtered output and the output of the decimator [8M]

7 a) Draw and explain the memory architecture of the TMS320C3X processor. [10M]

b) What are the major advantages of having on-chip memory? [6M]

Code No: RT32042 **R13** SET - 3

III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Show that the following system is nonlinear and time invariant. $y(n+2) + 2y(n) = x(n+1) + 2$	[4M]
	b)	State all properties of DFT	[4M]
	c)	Distinguish the canonic and non-canonic structures.	[4M]
	d)	Discuss the stability of the impulse invariant mapping technique.	[3M]
	e)	What is meant by aliasing? How to avoid it?	[4M]
	f)	List the basic characteristics of digital signal processor.	[3M]

PART –B

2	a)	Determine the frequency response, magnitude and phase responses and time delay of the systems given by $y(n) = x(n) - x(n-1) + x(n-2)$	[10M]
	b)	State and explain the transfer function of an LTI system.	[6M]
3	a)	Find the N-point DFT for $x(n) = a^n$ for $0 < a < 1$?	[8M]
	b)	Given x(n) = {1,2,3,4,4,3,2,1}, find X(k) using DIF FFT algorithm.	[8M]
4		Realize the following IIR system functions in the direct form I and II and also parallel form. $$H(z) = \frac{1}{(1+az^{-1})(1-bz^{-1})}$$	[16M]
5	a)	Design a digital Butterworth filter that satisfies the following constraint using bilinear transformation. Assume T=1sec. $$0.9 \le \left\|H\left(e^{jw}\right)\right\| \le 1 \qquad 0 \le w \le \frac{\pi}{2}$$ $$\left\|H\left(e^{jw}\right)\right\| \le 2 \qquad \frac{3\pi}{4} \le w \le \pi$$	[10M]

b) What is a Hamming window function? Obtain its frequency domain characteristics. [6M]

6 a) Draw the block diagram of a multistage decimator and explain it [8M]

b) Discuss the computationally efficient implementation of decimator in an FIR filter. [8M]

7 a) Draw and explain the major block diagram of the TMS320C3X. [10M]

b) Explain the function of Barrel Shifter in the digital signal processor. [6M]

Code No: RT32042 **R13** SET - 4

III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1 a) What is BIBO stability? What are the conditions for BIBO system? [4M]

b) How FFT is more efficient to determine DFT of sequence? [3M]

c) Distinguish between the methods of realization namely, block diagram representation and signal flow graph for implementing the digital filter transfer function. [4M]

d) What is the impulse invariant technique? [4M]

e) What are the drawbacks in multistage implementation? [3M]

f) Mention various generations of digital signal processors. [4M]

PART –B

2 a) Determine frequency, magnitude and phase responses and time delay for the system. [10M]

$$y(n) + \frac{1}{4}\, y(n-1) = x(n) - x(n-1)$$

b) Define the terms : linearity, time invariance and causality for a discrete time system. [6M]

3 a) Compute the FFT for the sequence x(n) = n+1 where N =8 using DIT algorithm [8M]

b) State and prove the periodicity property in DFT. [8M]

4 Realize the following IIR system functions in the direct form I and II and also parallel form. [16M]

$$H(z) = \frac{1}{(1-az^{-1})^2} + \frac{1}{(1-bz^{-1})^2}$$

5 a) What are the requirements for converting a stable analog filter into a stable digital filter? [6M]

b) The desired frequency response of a low pass filter is [10M]

$$H_d(e^{jw}) = \begin{cases} 1; & \frac{-\pi}{2} \le w \le \frac{\pi}{2} \\ 0; & \frac{\pi}{2} \le w \le \pi \end{cases}$$

Determine $h_d(n)$ for M =7 using a rectangular window.

6 a) How can sampling rate be converted by a rational factor M/L? [8M]

b) Draw and explain the polyphase structure of a interpolator. [8M]

7 a) Explain the purpose of six registers used in the TMS320C2X processor. [10M]

b) What are the limitations of pipelining in Digital Signal Processor? [6M]

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Code No: RT32042 **R13** SET - 1

III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) Find the power of the given signal below? [4M]

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b) Compare overlap-add method and overlap-save method [4M]

c) Compare direct form I and direct form II realization of IIR systems. [4M]

d) What conditions are to be satisfied by the impulse response of an FIR system in order to have a linear phase? [3M]

e) What is the need for multirate signal processing? [3M]

f) What are the differences between fixed type processors and floating type processors? [4M]

PART –B

2 a) Find the solution to the following linear constant coefficient difference equation [10M]

$$y(n) - \frac{3}{2}\, y\,(n-1) + \frac{1}{2} y(n-2) = \left(\frac{1}{2}\right)^n \; for \; n \geq \; 0$$

With initial conditions y(-1) = 4 and y(-2) = 10.

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3 a) Compute the DFT of the sequence x(n) = sin[nπ/4], where N=8 using DIT FFT algorithm [8M]

b) Determine the IDFT of the sequence [8M]

$$X(K) = (6, -\sqrt{2} - j4.8284, -2 + j2, \sqrt{2} - j0.8284, -2, \sqrt{2} + j0.8284, -2 - j2, -\sqrt{2} - j4.8284$$

4 Obtain the cascade and parallel realisation structures for the following signals. [16M]

$$H(z) = \frac{2(1 - z^{-1})(1 + \sqrt{2}z^{-1} + z^{-2})}{(1 + 0.5z^{-1}(1 - 0.9z^{-1} + 0.81z^{-2}))}$$

5 a) The desired frequency response of a low pass filter is

$$H_d(e^{jw}) = \begin{cases} e^{-j3w} & \frac{-3\pi}{4} \le w \le \frac{3\pi}{4} \\ 0 & elsewhere \end{cases}$$

[10M]

Determine $H(e^{jw})$ for M =7 using a rectangular window.

b) What are the effects of windowing? [6M]

6 a) Derive an expression for the spectrum of output signal of an decimator. [8M]

b) What are the applications of multirate system? [8M]

7 a) What is MAC? Explain its operation in detail. [10M]

b) What are the various addressing modes used in the TMS320C5X processor? [6M]

*****

Code No: RT32042 **R13** SET - 2

III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1 a) Show that the following systems are nonlinear and time invariant. [4M]
$y(n) – x(n)y(n-1) = x(n)$

b) Write computation efficiency of FFT over DFT. [3M]

c) What are the basic building blocks of realization structures? [4M]

d) Obtain the mapping formula for the impulse invariant transformation. [4M]

e) Write some examples of multirate digital systems. [3M]

f) What are the advantages of DSP processors in relation to general purpose processors? [4M]

PART –B

2 a) Determine the frequency response, magnitude and phase responses and time delay of the systems given by [10M]

$$y(n) - \frac{1}{2}y(n-1) = x(n)$$

b) Explain causality and stability of a linear time invariant system. [6M]

3 a) Find the DFT of the following sequence using FFT DIF? [8M]
X(n) = {1,2,3,5,5,3,2,1}

b) Compute the DFTs of the sequence $x(n) = 2^{-n}$, where N = 8 using DIT algorithm [8M]

4 Develop the cascade and parallel forms of the following causal IIR transfer functions. [16M]

$$H(z) = \frac{(3 + 5z^{-1})(0.6 + 3z^{-1})}{(1 - 2z^{-1} + 2z^{-2})(1 - z^{-1})}$$

5 a) Convert the analog filter to a digital filter whose system function is [10M]

$$H(s) = \frac{1}{(s+2)^2 + (s+1)}$$

Use bilinear transformation.

b) What is a Kaiser window? In what way is it superior to other window functions? [6M]

6 a) Draw the block diagram of a multistage interpolator and explain it [8M]

b) A one stage decimator is characterized by the following Decimator factor = 3. Anti-aliasing filter coefficients h(0) = -0.06 = h(4), h(1)=0.3 =h(3), h(2) =0.62. Given the data, s(n) with successive values [6,-2,-3,8,6,4,-2], calculate and list the filtered output and the output of the decimator [8M]

7 a) Draw and explain the memory architecture of the TMS320C3X processor. [10M]

b) What are the major advantages of having on-chip memory? [6M]

Code No: RT32042 **R13** SET - 3

III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A**is compulsory
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PART –A

1	a)	Show that the following system is nonlinear and time invariant. $y(n+2) + 2y(n) = x(n+1) + 2$	[4M]
	b)	State all properties of DFT	[4M]
	c)	Distinguish the canonic and non-canonic structures.	[4M]
	d)	Discuss the stability of the impulse invariant mapping technique.	[3M]
	e)	What is meant by aliasing? How to avoid it?	[4M]
	f)	List the basic characteristics of digital signal processor.	[3M]

PART –B

2	a)	Determine the frequency response, magnitude and phase responses and time delay of the systems given by $y(n) = x(n) - x(n-1) + x(n-2)$	[10M]
	b)	State and explain the transfer function of an LTI system.	[6M]
3	a)	Find the N-point DFT for $x(n) = a^n$ for $0 < a < 1$?	[8M]
	b)	Given x(n) = {1,2,3,4,4,3,2,1}, find X(k) using DIF FFT algorithm.	[8M]
4		Realize the following IIR system functions in the direct form I and II and also parallel form. $$H(z) = \frac{1}{(1+az^{-1})(1-bz^{-1})}$$	[16M]
5	a)	Design a digital Butterworth filter that satisfies the following constraint using bilinear transformation. Assume T=1sec. $$0.9 \le \left\|H(e^{jw})\right\| \le 1 \qquad 0 \le w \le \frac{\pi}{2}$$ $$\left\|H(e^{jw})\right\| \le 2 \qquad \frac{3\pi}{4} \le w \le \pi$$	[10M]

b) What is a Hamming window function? Obtain its frequency domain characteristics. [6M]

6 a) Draw the block diagram of a multistage decimator and explain it [8M]

b) Discuss the computationally efficient implementation of decimator in an FIR filter. [8M]

7 a) Draw and explain the major block diagram of the TMS320C3X. [10M]

b) Explain the function of Barrel Shifter in the digital signal processor. [6M]

Code No: RT32042 **R13** SET - 4

III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1 a) What is BIBO stability? What are the conditions for BIBO system? [4M]

b) How FFT is more efficient to determine DFT of sequence? [3M]

c) Distinguish between the methods of realization namely, block diagram representation and signal flow graph for implementing the digital filter transfer function. [4M]

d) What is the impulse invariant technique? [4M]

e) What are the drawbacks in multistage implementation? [3M]

f) Mention various generations of digital signal processors. [4M]

PART –B

2 a) Determine frequency, magnitude and phase responses and time delay for the system. [10M]

$$y(n) + \frac{1}{4}\, y(n-1) = x(n) - x(n-1)$$

b) Define the terms : linearity, time invariance and causality for a discrete time system. [6M]

3 a) Compute the FFT for the sequence x(n) = n+1 where N =8 using DIT algorithm [8M]

b) State and prove the periodicity property in DFT. [8M]

4 Realize the following IIR system functions in the direct form I and II and also parallel form. [16M]

$$H(z) = \frac{1}{(1-az^{-1})^2} + \frac{1}{(1-bz^{-1})^2}$$

5 a) What are the requirements for converting a stable analog filter into a stable digital filter? [6M]

b) The desired frequency response of a low pass filter is [10M]

$$H_d(e^{jw}) = \begin{cases} 1; & \frac{-\pi}{2} \le w \le \frac{\pi}{2} \\ 0; & \frac{\pi}{2} \le w \le \pi \end{cases}$$

Determine $h_d(n)$ for M =7 using a rectangular window.

6 a) How can sampling rate be converted by a rational factor M/L? [8M]

b) Draw and explain the polyphase structure of a interpolator. [8M]

7 a) Explain the purpose of six registers used in the TMS320C2X processor. [10M]

b) What are the limitations of pipelining in Digital Signal Processor? [6M]

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Code No: **R32043** **R10** **Set No. 1**

III B.Tech II Semester Regular/Supplementary Examinations, May/June - 2015
DIGITAL SIGNAL PROCESSING
(Comm to ECE and ECM)

Time: 3 hours **Max. Marks:75**

Answer any FIVE Questions
All Questions carry equal marks

*****

1 a) Define various elementary discrete time signals. Write notes on them and explain about their properties. [8]

b) Determine whether the following systems are time invariant or not a)y[n]=x[n]+nx[n-3] b)y[n]=sin(x[n]). [7]

2 a) State and prove the convolution theorem using DFT. [8]

b) Find the linear convolution of two sequences {1,0,2} and {1,1} using DFT. [7]

3 a) An 8 point sequence is given by x[n]={2,2,2,2,1,1,1,1} Find the DFT of the sequence using direct computation. [9]

b) Develop a radix-3 DIT FFT algorithm for evaluating the DFT for N=9. [6]

4 a) Discuss about different methods of realization of IIR systems and explain how the conversion can be made from direct form-I structure to direct form-II structure. [8]

b) Find the step response of the system whose impulse response is given by $h(n)=a^{-n}u(-n)$, $0<a<1$. [7]

5 a) Convert the following transfer function into digital filter using backward difference operator, $H(s)=\frac{3}{16+(s+0.5)^2}$ [8]

b) Explain about Frequency warping effect and suggest a remedy for it. [7]

6 a) Find and explain the frequency responses of rectangular and Hanning windows. [8]

b) Design a Linear phase low pass FIR filter with a cutoff frequency of $\pi/2$ rad/sec using frequency sampling technique. Take N=13. [7]

7 a) Define sampling. What is a down sampling operation and discuss about the Frequency response of a down sampling operation. [8]

b) Define a ramp sequence and sketch its interpolated and decimated versions with a factor of 3. [7]

8 Write short notes on the following

a) Multiplier and Accumulator [8]

b) Special addressing modes of dsp processors. [7]

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Code No: **R32043** **R10** **Set No. 2**

III B.Tech II Semester Regular/Supplementary Examinations, May/June - 2015
DIGITAL SIGNAL PROCESSING
(Comm to ECE and ECM)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
*****

1 a) Check whether the following systems are linear or not [8]
i)$y[n]=n^2x[n]$ ii)$y[n]=2x[n]+3$
b) Define a signal. Classify them with an example. [7]

2 a) Derive the relationship between DFT and z Transform. [8]
b) What is a twiddle factor? List out some of its properties. Explain the matrix representation of DFT and IDFT using twiddle factor. [7]

3 a) Explain the radix-2 DIT FFT algorithm and draw the butterfly diagram for 8-point DIT FFT. [10]
b) Compare DIT and DIF FFT algorithms. [5]

4 a) Compare FIR and IIR systems. [5]
b) Find the canonic forms of the system defined by the equation y[n]=x[n]-0.3x[n-1]-0.7x[n-2]+0.6y[n-1]+0.8y[n-2]. [10]

5 a) Design a chebyshev filter using Bilinear Transformation to meet the following specifications [8]
$0.3 \le |H(w) \le 1| \quad 0 \le w \le 0.1\pi$
$|H(w)| \le 0.1 \quad 0.4\pi \le w \le 2\pi$
b) Compare chebyshev and Butterworth approximations. [7]

6 a) Show that the magnitude response of FIR system is symmetric when impulse response is symmetric and N is odd. [8]
b) Design a FIR low pass filter with N=7 and cutoff frequency of π/4 rad/sec. [7]

7 a) A signal is defined as x[n] = sin (πn). Draw the original, interpolated and decimated signals by a factor of 3. [8]
b) Draw the block diagram of an Interpolator. Derive and Discuss about its frequency response characteristics. [7]

8 a) With a neat sketch explain the Internal architecture of TMS320C5X Processors. [9]
b) Explain about various addressing modes of a processor. [6]

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Code No: R32043 **R10** **Set No. 3**

III B.Tech II Semester Regular/Supplementary Examinations, May/June - 2015
DIGITAL SIGNAL PROCESSING
(Comm to ECE and ECM)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
*****

1 a) Determine whether the following signals are stable or not [8]
i)y[n]=8x[n-4] ii)x[n]=2^{-n}u[n] iii)y[n]=x^2[n-2]
b) What are the different operations that can be performed on a sequence? Explain them with an example. [7]

2 a) State and prove linearity, time shifting, and symmetry properties of DFS. [8]
b) A sequence is defined as x[n] = {1,-1,2,-2,3,-3}. Find the DFT. [7]

3 a) With a neat derivation explain the procedure to compute IDFT using Radix-2 FFT. [8]
b) Find the IDFT of the following sequence using DIT FFT of the sequence X(k) = {6, -j2, 2, j2}. [7]

4 a) Obtain the direct form I and II structures for the IIR System, $H(z)=\frac{4+3z+2z^2}{7+5z+z^2}$ [8]
b) Discuss about the basic elements used to construct the block diagram of a discrete time system. [7]

5 a) Design a Butterworth Low pass filter to meet the following specifications [10]
$0.89 \le |H(w)| \le 1 \quad 0 \le w \le w0.2\pi$
$|H(w)| \le 0.18 \qquad 0.3\pi \le w \le \pi$
b) Compare analog and digital filters. State the advantages of digital filters over the analog filters. [5]

6 a) Compare various windows used in the design of FIR filters. [7]
b) Design a low pass FIR filter with N=5, cutoff frequency of 200Hz and sampling time as 1ms using Fourier series method. [8]

7 a) Consider a signal x[n]={1,3,2,5,4,-1,-2,6,-3,7,8,9……} Show that the cascade of D down sampler and I up sampler is interchangeable only if D and I are co-prime. [8]
b) Explain about poly phase decomposition of FIR filters. [7]

8 a) What are programmable DSPs? Classify them. State the advantages of DSP processor over conventional microprocessors. [6]
b) Explain the VLIW architecture with its block diagram. State the advantages and disadvantages of VLIW architecture. [9]

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Code No: **R32043** **R10** **Set No. 4**

III B.Tech II Semester Regular/Supplementary Examinations, May/June - 2015
DIGITAL SIGNAL PROCESSING
(Comm to ECE and ECM)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

*****

1 a) Define stability of a system. Explain about BIBO stability criterion of a discrete system. [8]
b) i)Draw the even and odd parts of the following signals x[n]={5,4,3,2,1} [7]
ii)Check u[n]-u[n-6] is a power signal or not

2 a) Define DFS of a sequence and explain about exponential form and trigonometric forms. Derive the relation between two types of representations. [8]
b) A signal is defined as x[n]={1,2,3,-1,-2} Find the exponential form of DFS. [7]

3 a) A sequence is given by x[n]={1,2,3,4,4,3,2,1} Compute the 8-point DFT of x[n] by using radix-2 DIT FFT algorithm. [8]
b) Develop a DIF FFT algorithm for decomposing the DFT for N=3X2. [7]

4 a) What is an IIR system? Explain about Direct Form I and II structures for the IIR systems and also compare them. [8]
b) Realize the following transfer function using Direct Form II structure [7]
$H(z)=1+0.25z^{-1}+0.75z^{-2}$

5 a) Discuss about characteristics of analog Butterworth low pass filter and give its pole locations. Discuss about pole locations of digital chebyshev filter. [8]
b) Determine the order and the poles of the low pass Butterworth filter that has -3dB bandwidth of 500Hz and an attenuation of 40dB at 1000Hz. [7]

6 a) Design an FIR low pass filter using Hanning windows with pass band gain of 1dB, cutoff frequency of 400Hz, sampling frequency of 1 kHz. Assume the length of the impulse response as 7. [9]
b) Compare Hanning and Hamming windows [6]

7 a) Consider a sequence $x[n]=a^n u[n]$. i) Determine the spectrum of the signal. ii) The signal is applied to a decimator that reduces the sampling rate by a factor 2. Determine the output spectrum. [8]
b) Explain any two applications of Multi Rate signal processing [7]

8 a) Explain various interrupt structures supported by TMS320C5X Processor. [8]
b) What are the various on chip peripherals available in TMS320C5X Processor? Explain any two of them. [7]

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