Code No: RT22054 **R13** SET - 1

II B. Tech II Semester Regular Examinations, April/May - 2016
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1.	a)	Discuss about floating point representation	(4M)
	b)	Explain about Binary adder-substrator.	(4M)
	c)	What is LIFO? Discuss.	(4M)
	d)	What is BCD subtraction? Discuss.	(3M)
	e)	Define page fault and page replacement?	(4M)
	f)	Differentiate between full duplex and half duplex communication.	(3M)

PART –B

2.	a)	Discuss about the error detection using parity bit code with examples	(8M)
	b)	What is fixed point Representation? Explain with examples.	(8M)
3.	a)	What is instruction format? Discuss about the registers of basic computers.	(8M)
	b)	Discuss about the arithmetic logic shift unit with examples.	(8M)
4.	a)	Give the block diagram for register set in CPU.	(8M)
	b)	What is address sequencing? Discuss.	(8M)
5.	a)	How addition and subtraction is done for decimal numbers? Give the pictorial representation for adding two decimal numbers.	(8M)
	b)	Discuss about Booth's multiplication algorithm	(8M)
6.	a)	Discuss about the virtual memory? Discuss about the mapping of virtual address to memory table.	(8M)
	b)	Discuss about set-associative mapping.	(8M)
7.	a)	Discuss about parallel priority interrupt.	(8M)
	b)	Why does DMA have priority over the CPU When both request a memory transfer?	(8M)
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Code No: RT22054 **R13** SET - 2

II B. Tech II Semester Regular Examinations, April/May - 2016
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Discuss about BCD with examples. (3M)
   b) Differentiate between hardwired control and micro programmed control (4M)
   c) What is Reverse polish notation? Give examples. (4M)
   d) What is BCD Adder? Discuss. (4M)
   e) Discuss about bootstrap loader. (3M)
   f) What is asynchronous serial transfer? Discuss. (4M)

PART –B

2. a) Obtain the 9's compliment of the following eight-digit decimal numbers: 12349876; 00980100; 90009951 and 00000000 (4M)
   b) Perform the subtraction with the following unsigned decimal numbers by taking the 10's complement of the subtrahend (12M)
   i)5250-1321 ii) 1753-8640 iii) 20-100 iv) 1200-250

3. a) Explain about shift micro operations with examples. (8M)
   b) Write a short notes on Arithmetic micro operations. (8M)

4. Discuss about different CPU organizations with examples. (16M)

5. a) Explain how multiplication is done for floating point numbers with flow chart. (8M)
   b) Discuss about Booth's multiplication algorithm (8M)

6. a) Define Auxiliary memory? Discuss with neat diagrams. (8M)
   b) Explain about the procedure for mapping the virtual address in memory table. (8M)

7. a) What is priority interrupt? Discuss about daisy chaining priority interrupt. (8M)
   b) What is DMA? Explain with examples. (8M)
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Code No: RT22054 **R13** SET - 3

II B. Tech II Semester Regular Examinations, April/May - 2016
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1.	a)	What is two's compliment? Give examples	(3M)
	b)	What is Register Transfer? Discuss.	(4M)
	c)	Discuss about RISC instruction.	(4M)
	d)	What is Divide overflow? Discuss.	(3M)
	e)	Discuss about direct mapping.	(4M)
	f)	What is asynchronous data transfer? Discuss.	(4M)

PART –B

2.	a)	Obtain the 10's compliment of the following eight-digit decimal numbers: 123900; 090657; 100000 and 000000	(4M)
	b)	Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend i)11010-10000 ii) 11010-1101 iii) 100-110000 iv) 1010100-1010100	(12M)
3.	a)	Write the function table for arithmetic circuit? Discuss	(8M)
	b)	Design a 4-bit combinational circuit decrementer using 4 full adder circuits.	(8M)
4.		What is addressing modes? Discuss about different addressing modes with examples.	(16M)
5.	a)	Give flow chart for doing decimal division and also explain the sequence of operation of it.	(8M)
	b)	Explain how multiplication is done for floating point numbers with flow chart.	(8M)
6.	a)	What is associate memory? Explain with block diagram.	(8M)
	b)	Discuss about the mapping procedures of cache memory.	(8M)
7.		How the data transfer to and from peripherals is done? Discuss with neat diagrams and examples.	(16M)
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Code No: RT22054 **R13** SET - 4

II B. Tech II Semester Regular Examinations, April/May - 2016
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) What is one's compliment? Give examples (3M)
   b) Discuss about Three state bus buffers. (4M)
   c) What is relative addressing mode? Give example. (4M)
   d) Explain Array multifier. (4M)
   e) What is address space and memory space? Discuss. (4M)
   f) What is interrupted I/O? Discuss. (3M)

PART –B

2. a) Explain the functional units of a CPU. (8M)
   b) Explain Hamming code with example. (8M)

3. a) What is Register Transfer language? Discuss about the Register transfer with symbols and examples. (8M)
   b) What is Binary Adder? Discuss and also draw the 4-bit Binary adder? (8M)

4. How computer instructions are classified? List and explain about them with examples. (16M)

5. a) Discuss about Booth's multiplication algorithm (8M)
   b) Explain about the addition and subtraction for the floating point numbers with flow chart. (8M)

6. a) Discuss about Associative mapping with example. (8M)
   b) Discuss about the address mapping done by the paging. (8M)

7. a) What is handshaking? Discuss with neat diagrams. (8M)
   b) Draw the block diagram for asynchronous communication interface. (8M)
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Code No: RT22054 **R13** SET - 1

II B. Tech II Semester Supplementary Examinations, Dec – 2015.
COMPUTER ORGANIZATION
(Com. to CSE,IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) What are the error detection codes? Convert the decimal 225.225 to octal and hexadecimal (4M)
   b) Explain the different timing diagrams associated with buses (4M)
   c) Explain the stack organization (3M)
   d) Explain the operation of Associative memory (4M)
   e) What is virtual memory (3M)
   f) Draw a flow chart that describes the CPU-I/O channel communication (4M)

PART –B

2. a) Draw the functional diagram of a computer and explain each block (8M)
   b) By using the required parity generator/checker circuit, explain how parity checking canbe used for the error detection (8M)

3. a) Explain the instruction cycle with help of a flow chart (8M)
   b) What is register transfer language? Explain the basic symbols used in register transfer (8M)

4. a) With a neat diagram, explain the instruction pipeline processing in RISC architecture (8M)
   b) Evaluate the arithmetic statement X = (A+B) * (C+D) using a general register computer with three address, and two address instruction format (8M)

5. a) Multiply each of the following pairs of signed 2's complement numbers using booth algorithm and bit pairing of the multiplier (Assume A is the Multiplicand and B is the Multiplier). (8M)
   A=010111 B=110110
   A=110011 B=101100
   b) Draw and explain the division of floating point numbers (8M)

6. a) Explain mapping in segmented page memory unit with the help of a block diagram. What do you understand by translation look aside buffer (8M)
   b) What is the difference between isolated IO and memory mapped I/O? State the advantages and disadvantages of each (8M)

7. a) Draw and explain the 8x8 omega switch network (8M)
   b) A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at the rate of 2400 charaters per second. The CPU is fetching and executing instructions at an average rate of 1million instructions per second. By how much will the CPU be slowed down because of DMA transfer? (8M)

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Code No: RT22054 **R13** SET - 1

II B. Tech II Semester Regular Examinations, May/June - 2015
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

1. a) Find (1001101 - 10101001) using 1's complement?
   b) What is instruction cycle?
   c) Write the advantage of RISC over CISC?
   d) Draw the circuit diagram and Truth table for Full adder?
   e) Draw the hierarchy of memory? Why memory hierarchy is important in computer system?
   f) Differentiate between Synchronous and Asynchronous modes of data transfer?
   (3M+3M+4M+4M+4M+4M)

PART-B

2. a) Discuss three representations of Signed integers with suitable examples.
   b) Explain the components of the Computer system. (8M+8M)

3. a) List and explain the steps involved in the execution of a complete instruction
   b) What is Micro operation? Briefly explain the arithemetic micro operations? (8M+8M)

4. a) Explain the organization of registers.
   b) Explain how microinstructions execution takes place. (8M+8M)

5. a) Explain the issue involved with multiplication operation.
   b) Design 4-bit adder/Subtractor and explain its function. (8M+8M)

6. What is a mapping function? What are the ways the cache can be mapped? Explain in detail. (16M)

7. a) What is multiprocessor system? Explain the advantages of multi processors over uniprocessors
   b) Explain the functions of typical input-output interface. (8M+8M)
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Code No: RT22054 **R13** SET - 2

II B. Tech II Semester Regular Examinations, May/June - 2015
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

1. a) What are 2's Compliment? Give its Significance?
   b) What is interrupt? Give the steps for handling interrupt?
   c) Compare RISC and CISC?
   d) Realize full adder using two half adders and logic gate?
   e) What is Auxiliary memory?
   f) What are different forms of parallelism? (4M+4M+4M+4M+3M+3M)

PART-B

2. a) Explain the functional architecture of the computer system.
   b) Discuss the concept of compliments used to represent signed numbers. (8M+8M)

3. a) What is instruction cycle? Briefly explain with the help of state diagram?
   b) Briefly explain the arithmetic logic shift unit (8M+8M)

4. a) Explain the various addressing modes with examples.
   b) Explain the basic organization of microprogrammed control unit (8M+8M)

5. a) Design carry look ahead adder and explain its function.
   b) Derive and explain an algorithm for adding and subtracting 2 floating point binary numbers (8M+8M)

6. a) Explain the Address Translation in Virtual Memory
   b) Explain different types of mapping functions in cache memory (8M+8M)

7. a) How data transfers can be controlled using handshaking technique?
   b) Explain organization of multiprocessor system with neat sketch. (8M+8M)
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Code No: RT22054 **R13** SET - 3

II B. Tech II Semester Regular Examinations, May/June - 2015
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

Part A

1. a) What is parity? Give its significance?
   b) What is one address, two address and three address instruction formats?
   c) What is Register Indirect Addressing mode? Give an example?
   d) Draw the circuit diagram and Truth table for half adder?
   e) What is Cache memory? Mention its advantages?
   f) What is the use of priority interrupt? (3M+4M+4M+4M+4M+3M)

PART-B

2. a) Describe the connections between the processor and memory with a neat structure diagram
   b) Find 2's complement of the following
   i) 10010 ii) 111000 iii) 0101010 iv) 111111 (8M+8M)

3. a) Explain the Memory reference instructions? Give examples?
   b) List and explain the shift micro operations? (8M+8M)

4. a) Explain micro instruction sequencing in detail.
   b) With a neat diagram explain the internal organization of a processor. (8M+8M)

5. a) Explain hardware implementation of Binary multiplier with example.
   b) Discuss decimal arithmetic operations (8M+8M)

6. a) Explain about associative memory
   b) Explain internal organization of memory chips. (8M+8M)

7. a) With a neat sketch explain the working principle of DMA
   b) Explain the interconnection structure for multiprocessor systems (8M+8M)
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Code No: RT22054 **R13** SET - 4

II B. Tech II Semester Regular Examinations, May/June - 2015
COMPUTER ORGANIZATION
(Com. to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART-A

1. a) What Sign magnitude representation? Give an example?
b) Draw the structure of basic computer system?
c) What is addressing mode? List any four Addressing modes?
d) Draw the diagram for 4-bit adder?
e) What is Virtual memory? Why it is significant?
f) What is DMA? Write its Advantages? (4M+3M+4M+3M+4M+4M)

PART-B

2. a) Discuss about fixed point and floating point representations
b) What are functions of ALU and explain. (8M+8M)

3. a) What is RTL? Explain with suitable examples? What is its significance Instructions?
b) What is Interrupt? Explain Input output interrupts? (8M+8M)

4. a) Explain different addressing modes.
b) Mention the advantages and disadvantages of microprogrammed control hardwired control (8M+8M)

5. a) Explain division algorithm with example.
b) Explain Booth Multiplication algorithm with example. (8M+8M)

6. a) Analyze the memory hierarchy in terms of speed, size and Cost.
b) Design 64k X 16 memory chip using 16k X 8 memory chips (8M+8M)

7. a) What are handshaking signals. Explain the handshake control of data transfer during input and output operation
b) What is parallel processing? Explain any parallel processing mechanism. (8M+8M)
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Code No: **R41021** **R10** **Set No. 1**

IV B.Tech I Semester Supplementary Examinations, May/June - 2014

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time : 3 hours **Max. Marks: 75**

Answer any Five Questions

All Questions carry equal marks

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1 a) With the help of a diagram, explain how data is transferred between the processor and main memory. [8]
b) Explain floating point representation with examples. [7]

2 a) Explain in detail about shift micro operations. [8]
b) Draw and explain the bus structure for the data transfer between various registers and the common bus. [7]

3 a) Explain about different types of instruction formats with examples. [8]
b) What is effective address? How to find the effective address in each addressing mode? Give examples [7]

4 a) Explain about the basic organization of a micro programmed control unit. [8]
b) With the help of a diagram, explain about control memory and its associated hardware. [7]

5 a) What is virtual memory? How to translate the virtual address into physical address? [8]
b) Draw the memory hierarchy. Compare the speed, size and cost of these memories. [7]

6 a) Explain the modes of data transfer in DMA. [8]
b) Explain in detail about Asynchronous data transfer. [7]

7 a) Explain about RISC pipe line. [8]
b) Distinguish between Array processing and Vector processing. [7]

8 a) Discuss the characteristics of multi processors. [8]
b) Explain about inter processor arbitration. [7]

Code No: **R41021** **R10** **Set No. 2**

IV B.Tech I Semester Supplementary Examinations, May/June - 2014

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time : 3 hours **Max. Marks: 75**

Answer any Five Questions
All Questions carry equal marks

*****

1 a) With the help of a neat block diagram, explain about the functional units of a computer. [8]
b) Discuss about the factors that influence the performance of a computer. [7]

2 a) Explain about the hardware implementation of logic micro operation for AND, OR and XOR gates [8]
b) Explain about Register Transfer Language. [7]

3 a) What is an addressing mode? Explain about different types of addressing modes with examples. [8]
b) Consider a computer that has a byte-addressable memory organized in 32-bit words according to the big-endian scheme. A program reads input characters entered at a key board and stores them in successive byte locations, starting at location 1000. Show the contents of the memory after the name "Computer Organization" has been entered. [7]

4 a) Explain how control signals are generated in a Hard wired control unit. [8]
b) Explain about address sequencing in control memory. [7]

5 a) Discuss the features of various types of Read Only Memories. [8]
b) Distinguish between 'Write-Back' and 'Write-Through' mechanisms in cache memory organization. [7]

6 a) What is an interrupt? Explain about priority interrupts. [8]
b) Distinguish between a 'Sub-Routine' and an 'Interrupt –Service-Routine'. [7]

7 a) Explain about Arithmetic pipeline. Also discuss its influence on the performance of a computer. [8]
b) What is an Array processor? Discuss the major characteristics of Array processors. [7]

8 a) Explain about various types of interconnection structures in Multi-processors. [8]
b) List the features of shared memory Multi processors. [7]

Code No: **R41021** **R10** **Set No. 3**

IV B.Tech I Semester Supplementary Examinations, May/June - 2014

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time : 3 hours **Max. Marks: 75**

Answer any Five Questions

All Questions carry equal marks

*****

1	a)	Write the algorithm for floating point arithmetic subtraction.	[8]
	b)	Explain about various functional units of a computer.	[7]
2	a)	Differentiate between 'Interrupt Cycle' and 'Instruction Cycle'. Draw the flow chart for Instruction Cycle.	[8]
	b)	Explain about register transfer operations.	[7]
3	a)	Explain the evaluation of arithmetic expressions using stack.	[8]
	b)	Discuss the features of Reduced Instruction Set Computers.	[7]
4	a)	Explain about address sequencing in control memory.	[7]
	b)	Explain about hard wired control for generating control signals.	[8]
5	a)	Explain how information is stored and retrieved from a Dynamic RAM cell.	[7]
	b)	Explain the organization of virtual memory.	[8]
6	a)	How is data transferred between memory and I/O devices using DMA?	[8]
	b)	Explain about Input-Output interface.	[7]
7	a)	Explain how instruction pipelining improves the performance of a computer. Give an example	[8]
	b)	Explain about vector processing.	[7]
8	a)	Draw and explain about time shared common bus interconnection structure.	[8]
	b)	List the characteristics of Multi-processors.	[7]

Code No: **R41021** **R10** **Set No. 4**

IV B.Tech I Semester Supplementary Examinations, May/June - 2014

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time : 3 hours **Max. Marks: 75**

Answer any Five Questions

All Questions carry equal marks

*****

1 a) Write the algorithm for floating point arithmetic multiplication. [8]
b) Write and explain about the performance equation of a computer. [7]

2 a) Draw and explain the flowchart of an instruction cycle. [8]
b) Explain about 'Register Transfer Language'. [7]

3 a) How to convert an infix expression into post-fix form using stack? [7]
b) Explain about data transfer, data manipulation and program control instructions with examples. [8]

4 a) Distinguish between hard wired control and micro programmed control. [8]
b) Explain about the design of a control unit. [7]

5 a) How are 'Read' and 'Write' operations performed on a static RAM cell? [8]
b) Explain the terms 'Hit Ratio' and 'Miss Penalty' in the context of cache memory. [7]

6 a) How is data transferred between Memory and I/O devices using DMA? [8]
b) What is an interrupt? Explain about Priority Interrupts. [7]

7 a) List the characteristics of Array Processors. [8]
b) Draw the space time diagram for a 'Five-Segment Pipeline' showing the time it takes to complete 8 tasks. [7]

8 a) Explain about Hypercube interconnection structure. [8]
b) Discuss the features of shared memory Multi-processors. [7]

Code No: R22054 **R10** SET - 1

II B. Tech II Semester Supplementary Examinations January – 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Describe the interconnection structure of a computer?
   b) Explain format of assembly language?

2. Explain about CPU organization?

3. Write short notes on the following:
   a) Register transfer language
   b) Instruction formats
   c) Addressing modes
   d) Reduced Instruction Set Computer

4. Explain the Hardwired control and Micro programmed control. Also explain their advantages and disadvantages?

5. a) Explain Booth's algorithm from its theoretical basis?
   b) Multiply 11101_2 with 10101_2 using Booth's algorithm.

6. a) Discuss about address translation in paging.
   b) How does page size effects storage utilization and effective memory data transfer rate?

7. Explain the following:
   a) Asynchronous Serial Transfer
   b) Asynchronous Communication Interface.

8. a) What is meant by instruction pipeline? Explain.
   b) Explain the following with related to the instruction pipeline
      i) Pre-fetch target instruction
      ii) Branch target buffer

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Code No: R22054 **R10** SET - 2

II B. Tech II Semester Supplementary Examinations January – 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain about instruction set architecture design?
   b) Explain about instruction format?

2. Explain about memory sub-system organization?

3. a) Explain about hardware description language?
   b) Explain about Micro operations?

4. a) Explain why hardwired control unit is faster than micro programmed control unit.
   b) What is microinstruction? How do we reduce number of microinstructions?

5. a) Find the output binary number after performing the arithmetic operation using 1's complement representation.
      i) $111.01_2 + 10.111_2$
      ii) $110.11_2 - 111.01_2$
   b) Explain steps involved in the addition of numbers using 2's complement notation?

6. a) Explain how the Bit Cells are organized in a Memory Chip.
   b) Explain the organization of a 1K x 1 Memory with a neat sketch.

7. a) Explain programmed I/O in detail.
   b) Explain interrupt initiated I/O in detail.

8. a) List and explain different interconnection structures used in multiprocessors?
   b) Explain system bus structure for multiprocessors with a neat sketch.
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Code No: R22054 **R10** SET - 3

II B. Tech II Semester Supplementary Examinations January – 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain 8085 microprocessor instruction set architecture?
   b) Explain about addressing modes?

2. Explain about I/O sub-system organization and interfacing?

3. a) What are micro operations? Explain
   b) Explain the instructions used in Register Transfer Language?

4. a) Compare the hardwired control with micro programmed control in terms of complexity of the instruction set, ease of modification and clock speed.
   b) Explain about micro sequence control unit design?

5. a) Find the output binary number after performing the following arithmetic operations
      i) $111.01_2 + 10.111_2$
      ii) $11.01_2 + 110.11_2$
      iii) $110.11_2 - 111.01_2$
   b) Explain about specialized arithmetic hardware?

6. a) Differentiate between single versus two-level caches.
   b) Elaborate on Pentium Cache Organization.

7. a) What is Direct Memory Access? Explain the working of DMA.
   b) Discuss about I/O channel architecture.

8. a) Explain communication in multi processor systems?
   b) What is cache coherence? Explain its importance.

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Code No: R22054 **R10** SET - 4

II B. Tech II Semester Supplementary Examinations January – 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) What are the levels of programming language? Explain.
   b) What is instruction set? Explain with an example?

2. a) Explain about memory interfacing?
   b) Explain about I/O interfacing?

3. a) Explain about Register Transfer Language?
   b) Explain about programming through VHDL with a sample program?

4. a) Give the typical horizontal and vertical microinstruction formats.
   b) Describe how microinstructions are arranged in control memory and how they are interpreted.

5. a) How subtraction is done on the binary numbers represented in one's complement notation give an examples?
   b) What do you mean by r's complement?

6. a) Compare and contrast asynchronous DRAM and synchronous DRAM.
   b) Compare and contrast direct and associative mapping techniques.

7. a) How would CPU handles multiple devices. Explain with different techniques available?
   b) Discuss the characteristics of Intel 8259A interrupt controller.

8. a) Explain RISC pipeline?
   b) Explain different types of parallel processors?
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Code No: R22054 **R10** SET - 1

II B. Tech II Semester Regular Examinations August - 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain the instruction set architecture of 8085.
   b) What addressing mode is used by the following instructions for the relatively simple CPU?
   i) MVAC ii) CLAC iii) JMPZ Γ (8M+7M)

2. a) Explain and draw neat timing diagrams for Memory Read and Memory Write operations.
   b) Design an interface for an input device which binary address 10101010.Its computer system uses isolated I/O. (7M+8M)

3. a) Explain briefly about the shift micro operation.
   b) Write the RTL statements for the following transitions. All registers are 1-bit wide.
   i) IF α = 1 THEN copy X to W and copy Z to Y
   ii) IF α = 0 THEN copy X to W (8M+7M)

4. a) Distinguish between Hardwired control unit and Micro programmed Control unit.
   b) Draw and explain briefly about Fetch and Decode cycles for the Simple CPU. (5M+10M)

5. Design the RTL code for the shift-add multiplication UV<--X.Y for X=9 and Y=14. (15M)

6. a) Distinguish between Logical address and Physical address with an example.
   b) A computer system using the relatively simple CPU is to include a 1k associative cache with a line size of 2 bytes.
   i) How many bits are in each location of the cache?
   ii) What mask value is needed for the associative memory? (7M+8M)

7. a) Distinguish between Synchronous data transfer and Asynchronous data transfer.
   b) What is an Interrupt? Explain about different types of Interrupts. (5M+10M)

8. a) Explain the formats used by the 32-bit SPARC CPU.
   b) Explain Flynn's Classification of parallel computers. (7M+8M)
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Code No: R22054 **R10** SET - 2

II B. Tech II Semester Regular Examinations August - 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain about various addressing modes in Assembly Language Instructions.
   b) Write the instruction code formats for Assembly language programs and Machine code to calculate A=B+C for two-operand and zero-operand instructions (8M+7M)

2. a) Explain about the different types of Memory Chips.
   b) Construct a 16 X 2 memory subsystem constructed from two 8 X 2 ROM chips with high-order interleaving. (7M+8M)

3. Explain VHDL file to implement modulo 6 counter using high level of abstraction. (15M)

4. a) Explain the generic Micro instruction Formats.
   b) Explain Micro Sequencer for the relatively simple CPU with micro subroutines. (5M+10M)

5. a) Construct a 3 × 3 multiplexer using a Carry-Save Adder.
   b) Explain about overflow generation in unsigned two's complement Addition. (8M+7M)

6. a) Differentiate Cache memory Vs Virtual memory.
   b) Explain about External fragmentation in physical memory caused by Segmentation. (8M+7M)

7. a) Explain the concept of Handshaking technique.
   b) Explain I/O Processor with a neat diagram. (5M+10M)

8. Explain Instruction Pipelines and its conflicts with Examples. (15M)
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Code No: R22054 **R10** SET - 3

II B. Tech II Semester Regular Examinations August - 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain about Data transfer instructions in Assembly Language Instructions.
   b) What addressing mode is used by the following instructions for the 8085 micro processor?
   i) SPHL ii) CMC iii) JUMP Γ (8M+7M)

2. a) Distinguish between SRAM and DRAM.
   b) Explain the CPU internal Organization. (7M+8M)

3. a) Draw the State diagram for modulo 6 counter.
   b) What is a hardware description language? Explain the features of VHDL. (10M+5M)

4. Draw and explain the Generic Hardwired Control unit. (15M)

5. a) Show the Wallace tree to perform 6 × 6 Multiplication.
   b) What is the result of the following operations on unsigned non-negative numbers using 1's complement.
   i) 1011 0100 – 0111 0111
   ii) 1000 1011 + 0111 0100
   iii) 10101.101+11011.001 (8M+7M)

6. a) Explain about Locality of Reference.
   b) Explain cache memory with Direct Mapping technique. (5M+10M)

7. a) Explain about Daisy Chaining.
   b) Explain incorporating Direct Memory Access into a computer system. (5M+10M)

8. a) Compare RISC and CISC processors.
   b) Explain Multiprocessor system inter connection N/w topologies. (7M+8M)
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Code No: R22054 **R10** SET - 4

II B. Tech II Semester Regular Examinations August - 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain about Instruction Set Architecture Design.
   b) Write a program for relatively Simple CPU to add the ten values in memory locations 1001H through 100AH and store the result in memory location 1000H.Assume the result will always be less than 256. (8M+7M)

2. a) Show the internal two dimensional configuration of a 32 × 2 Memory chip.
   b) Show how the following values are stored in memory in big endian and little endian formats. Each value starts at location 22H. i) 0927H ii) 5551212H (8M+7M)

3. a) Explain the operation of Toll Booth Controller.
   b) Show the hardware to implement shl(x) micro-operation. X consists of four D flip-flops. Each micro-operation occurs when $\alpha = 1$. (8M+7M)

4. a) Explain briefly about micro sequencer operations.
   b) Show the logic to generate the control signals for data register, address register and instruction register of the relatively simple CPU. (8M+7M)

5. Explain the Hardware implementation of Booth's multiplication algorithm. Discuss with an example and draw the flow chart. (15M)

6. What is paging? Explain the conversion of logical address to physical address using the page table. (15M)

7. a) Distinguish between memory mapped I/O and I/O mapped I/O.
   b) Explain the internal configuration of UART. (5M+10M)

8. a) Explain RISC processors briefly. Mention its advantages.
   b) Explain about SIMD organization with neat sketch. (8M+7M)
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